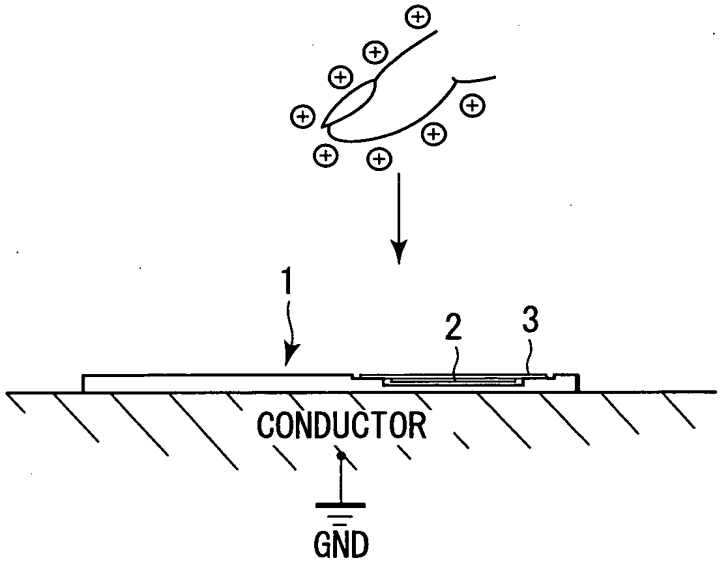


FIG. 1A

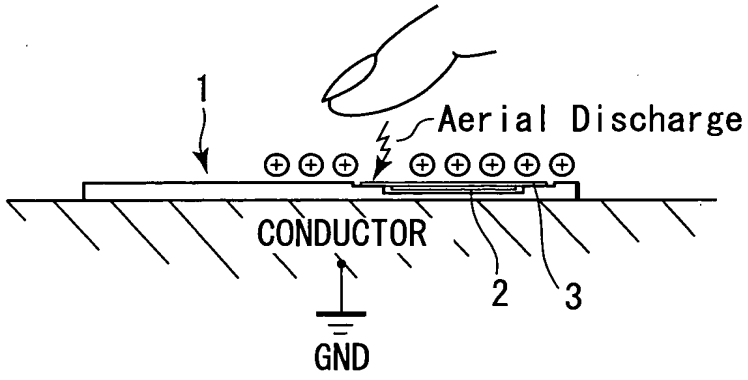


FIG. 1B

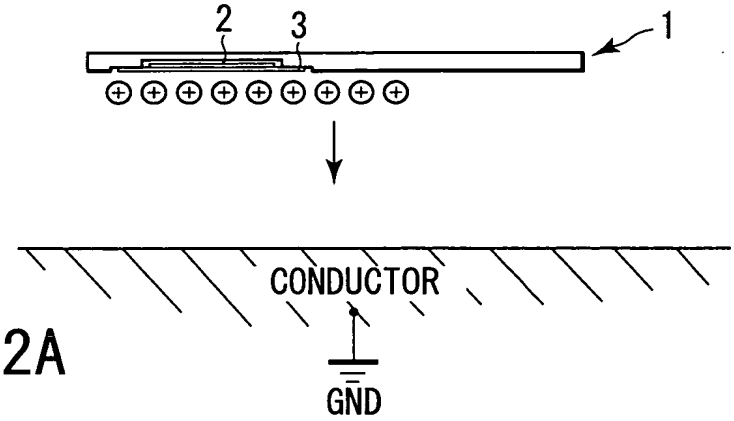


FIG. 2A

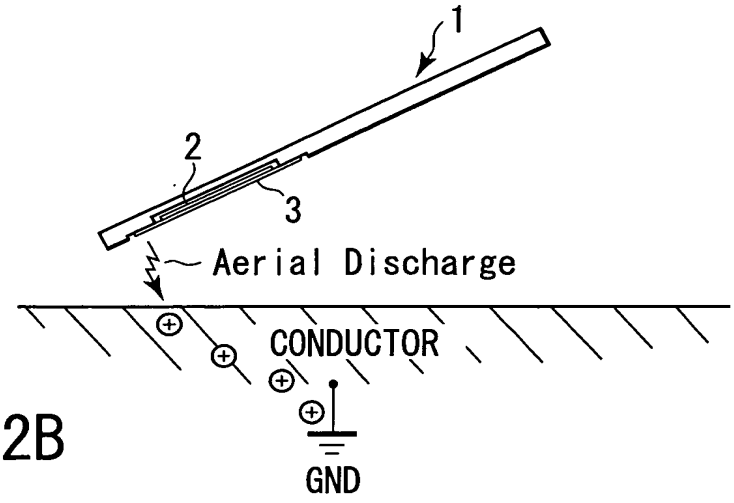


FIG. 2B

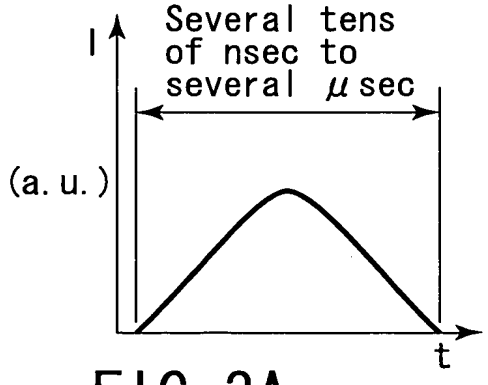


FIG. 3A

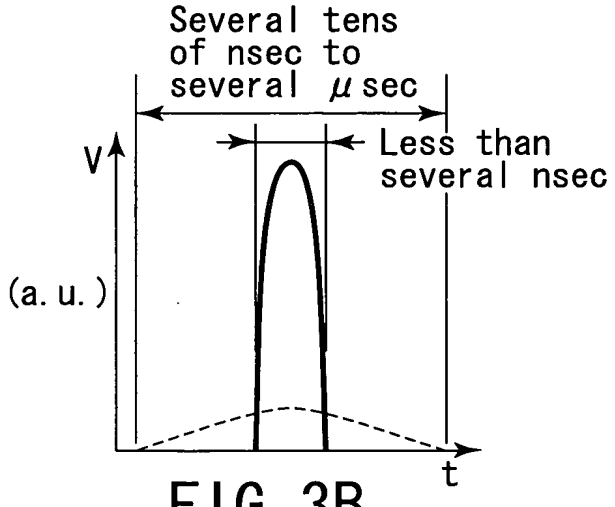


FIG. 3B

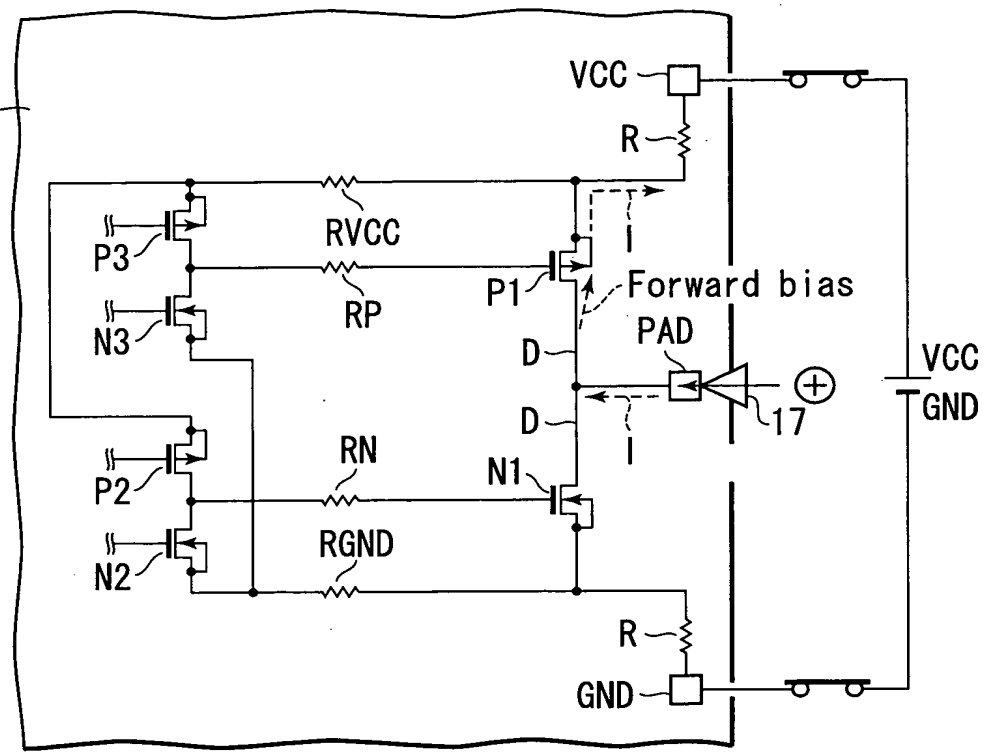

2
VCC
R
RVCC
P3
RP
P1
Forward bias
N3
PAD
D
VCC
GND
17
D
RN
P2
N1
RGND
N2
R
GND

FIG. 4A

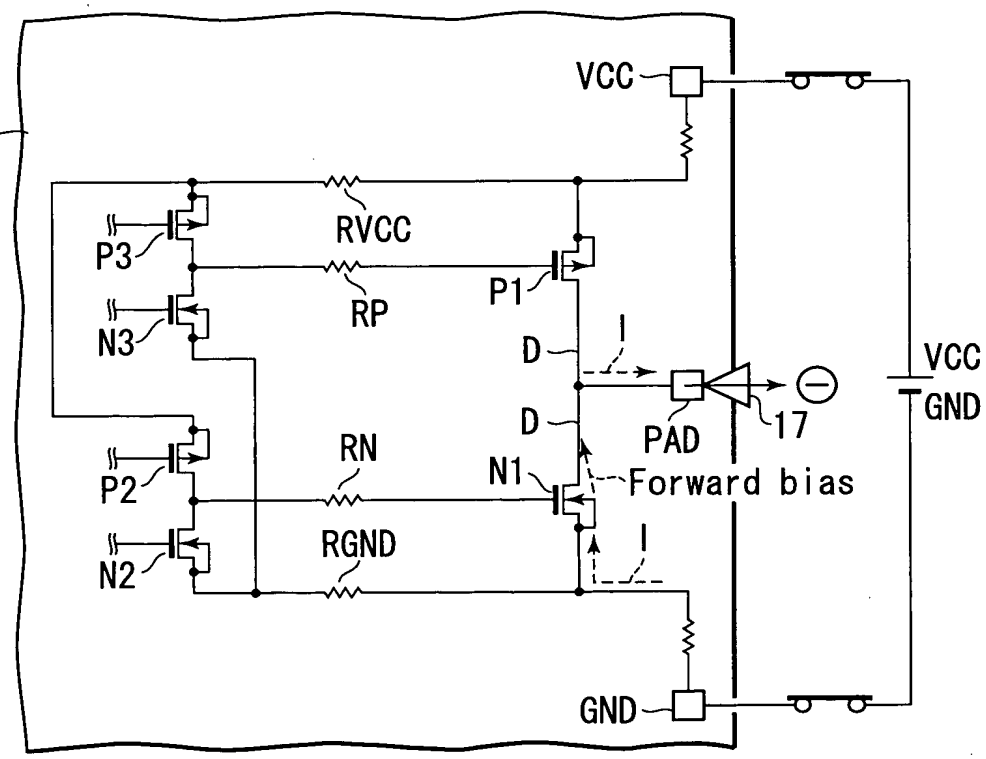

2
VCC
RVCC
P3
RP
P1
N3
D
VCC
GND
D
PAD
17
RN
P2
N1
Forward bias
RGND
N2
GND

FIG. 4B

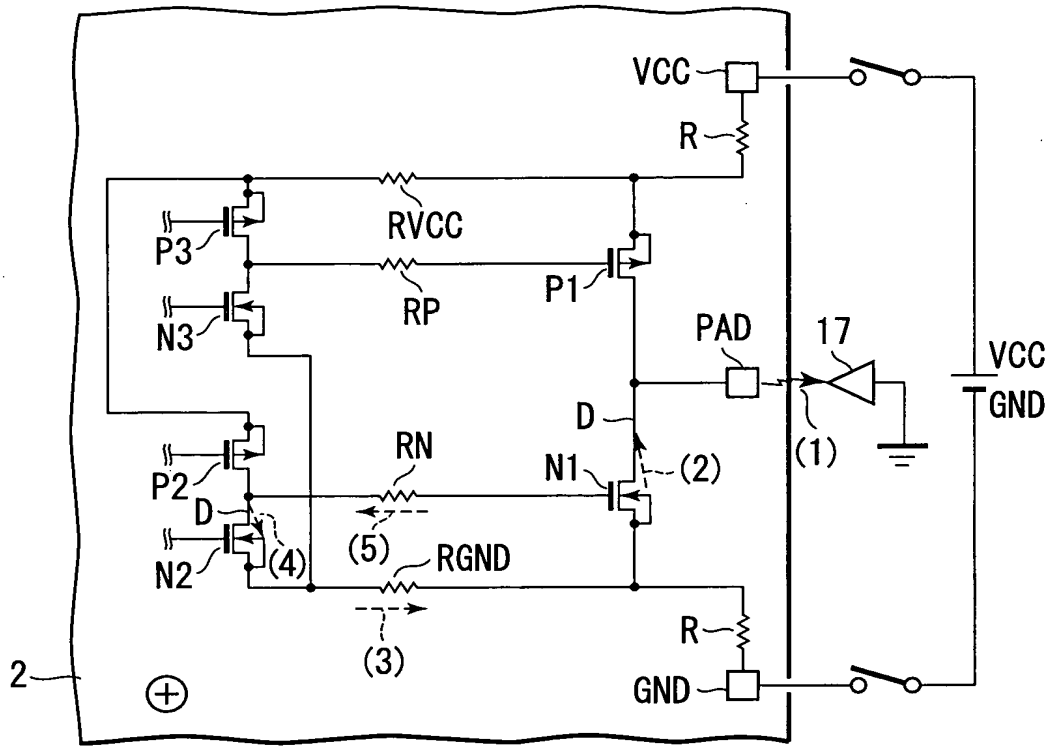

VCC
R
RVCC
P3
RP
P1
N3
PAD
17
VCC
GND
D
RN
N1
(2)
(1)
P2
D
(5)
RGND
N2
(4)
(3)
R
2
GND

FIG. 5A

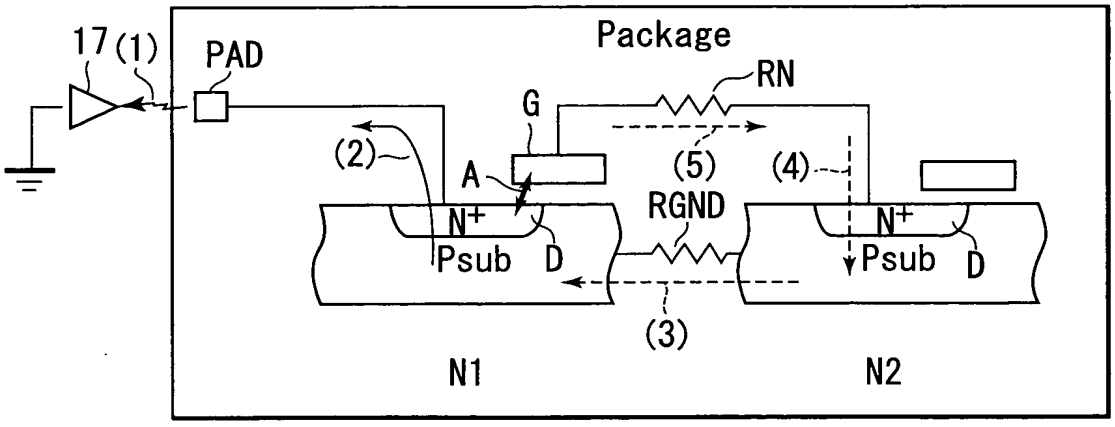
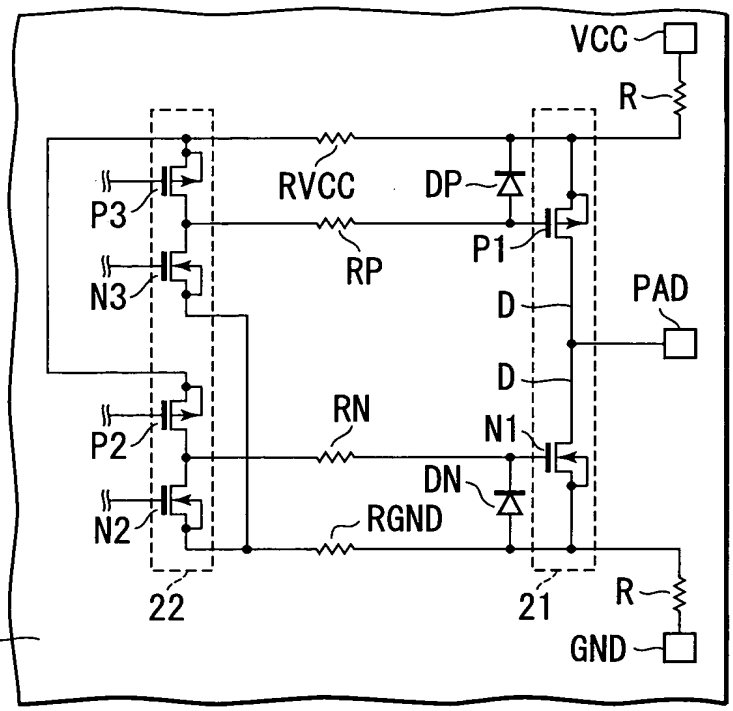

17
(1)
PAD
Package
RN
G
(2)
(5)
(4)
A
RGND
N+
N+
Psub
D
Psub
D
(3)
N1
N2

FIG. 5B

FIG. 6A


VCC
R
RVCC
DP
P3
P1
RP
N3
D
PAD
D
RN
P2
N1
DN
N2
RGND
22
21
R
2
GND

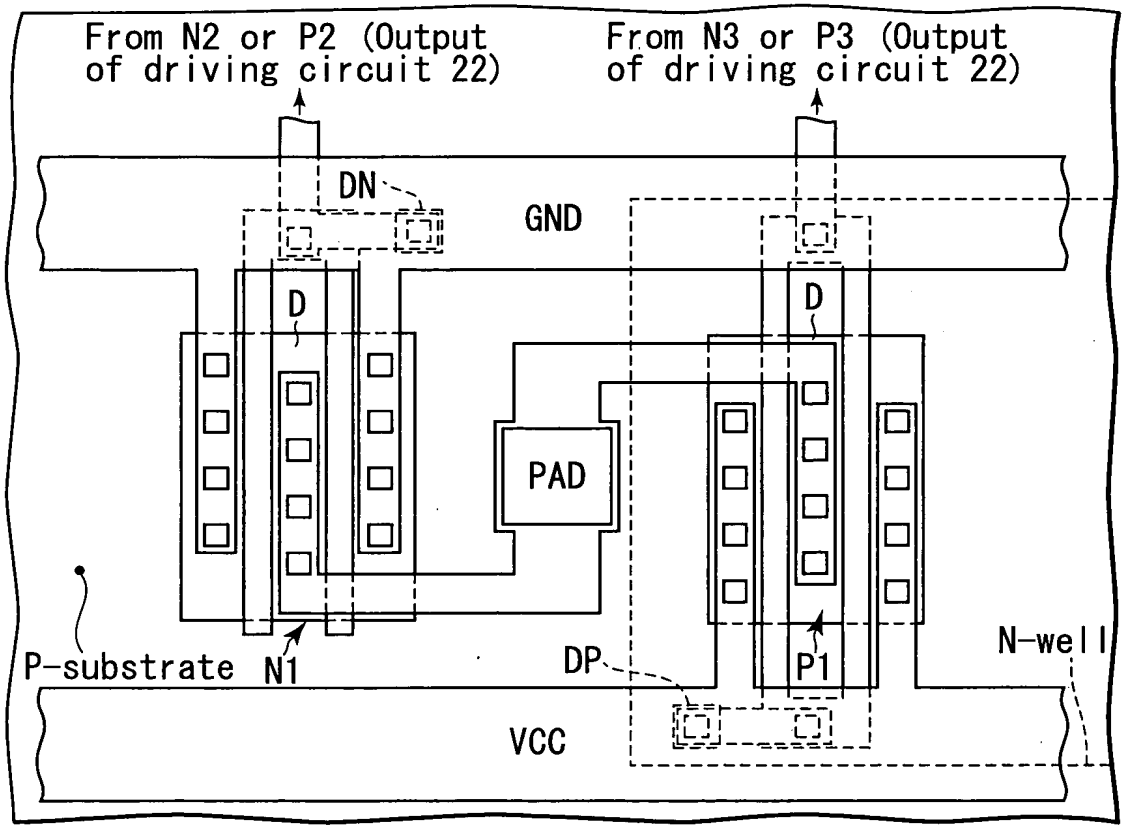

From N2 or P2 (Output of driving circuit 22)
From N3 or P3 (Output of driving circuit 22)
DN
GND
D
D
PAD
P-substrate
N1
DP
P1
N-well
VCC

FIG. 6B

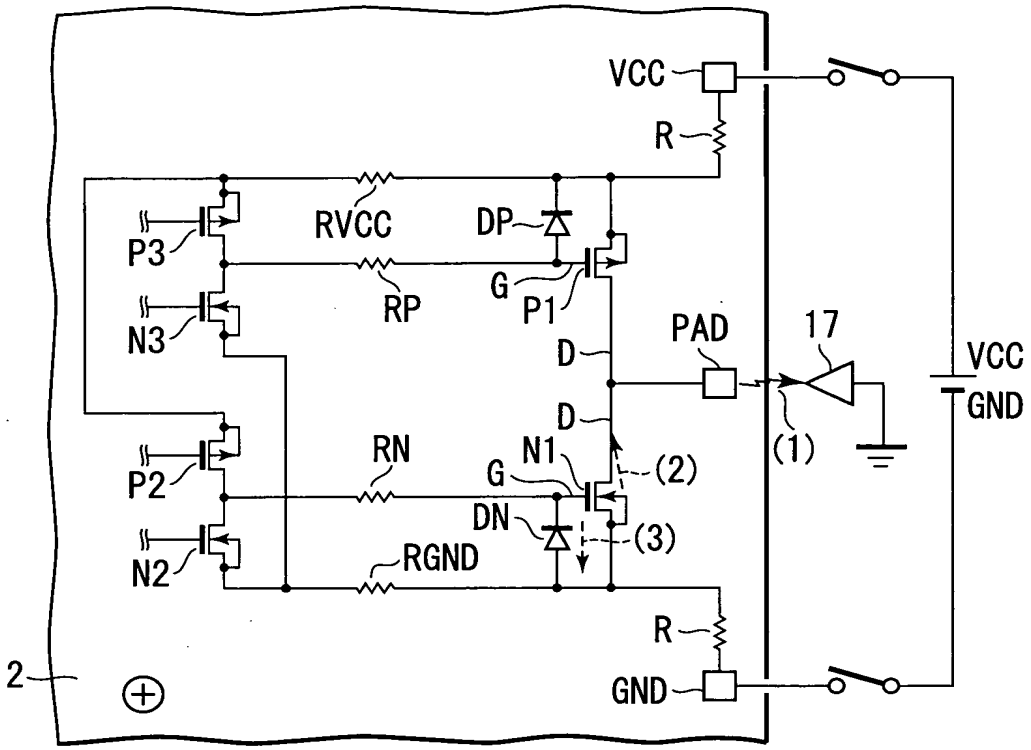

VCC
R
RVCC
DP
P3
G
P1
RP
N3
PAD
17
D
VCC
GND
D
(1)
RN
N1
(2)
P2
G
DN
(3)
N2
RGND
R
2
GND

FIG. 7A

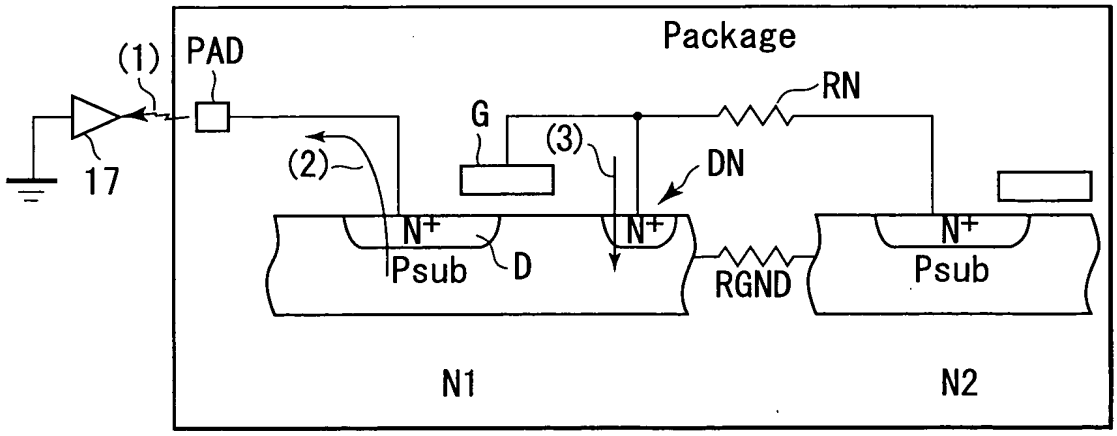

Package
(1)
PAD
RN
G
(3)
(2)
DN
17
N+
N+
N+
Psub
D
RGND
Psub
N1
N2

FIG. 7B

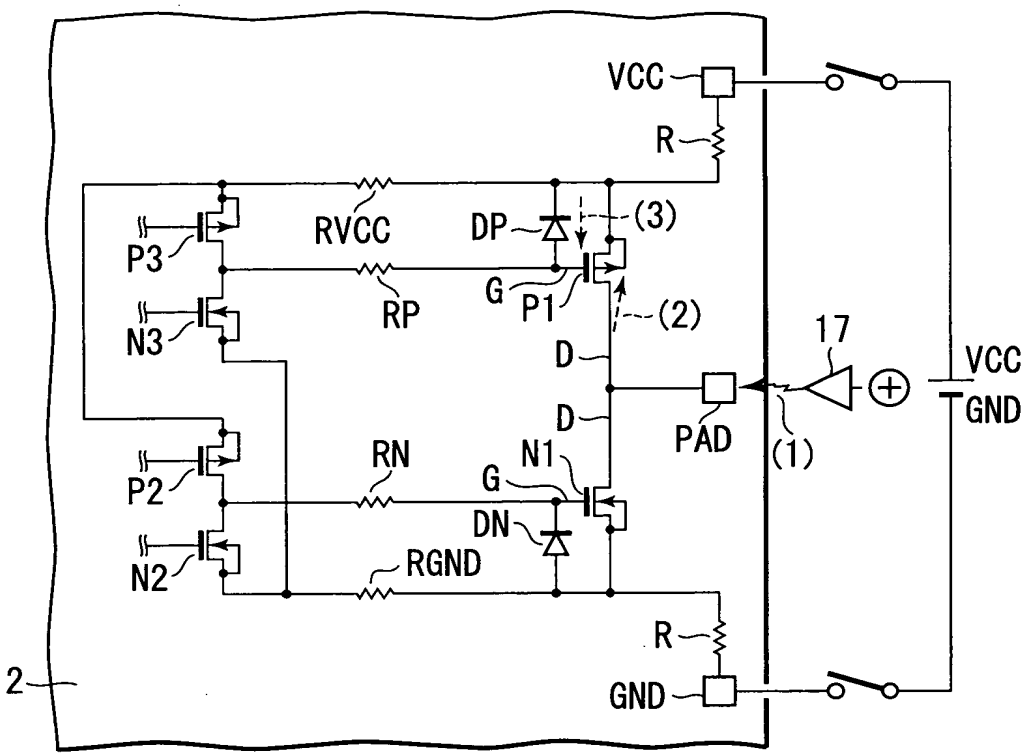

VCC
R
RVCC
DP
(3)
P3
G
P1
RP
(2)
N3
D
17
VCC
GND
D
PAD
(1)
P2
RN
N1
G
DN
N2
RGND
R
2
GND

FIG. 8A

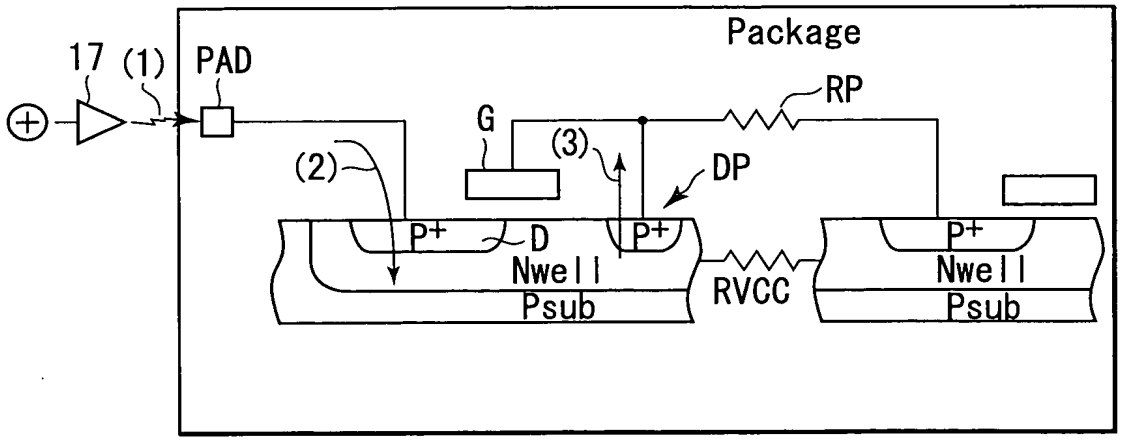

Package
17
(1)
PAD
RP
G
(3)
(2)
DP
P+
D
P+
P+
Nwell
Psub
RVCC
Nwell
Psub

FIG. 8B

FIG. 9

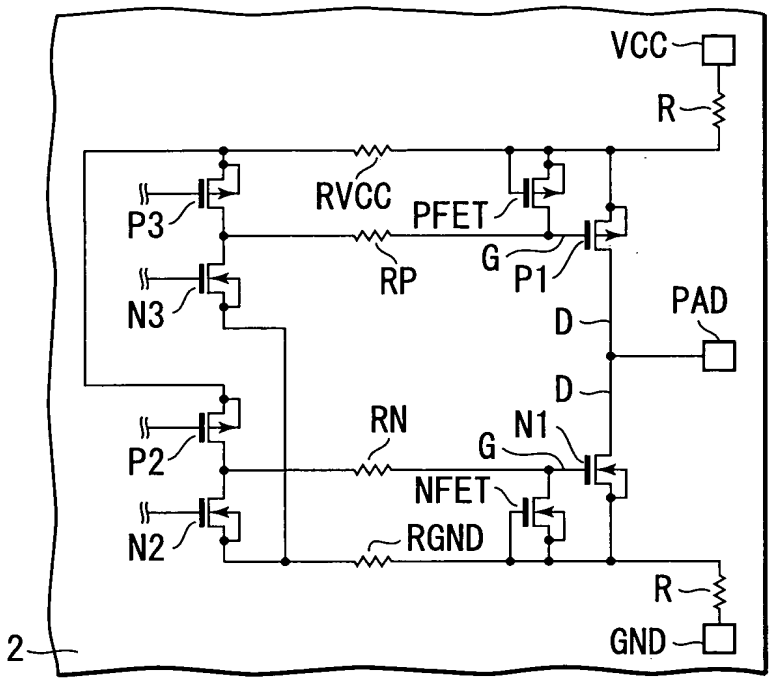
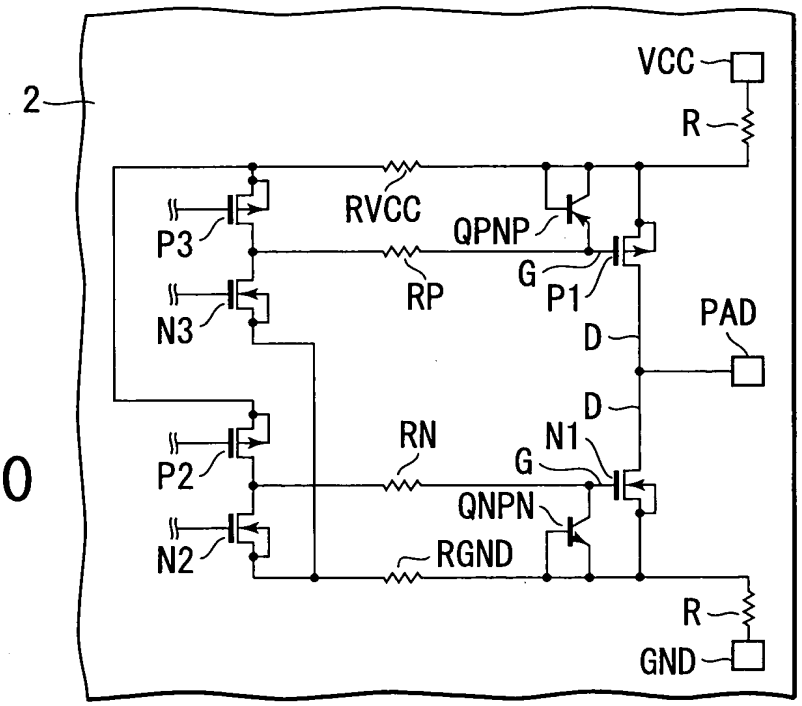

VCC
R
RVCC
PFET
P3
RP
G
P1
N3
PAD
D
D
RN
N1
G
P2
NFET
N2
RGND
R
GND
2

FIG. 10


2
VCC
R
RVCC
QPNP
P3
G
RP
P1
N3
PAD
D
D
RN
N1
G
P2
QNPN
N2
RGND
R
GND

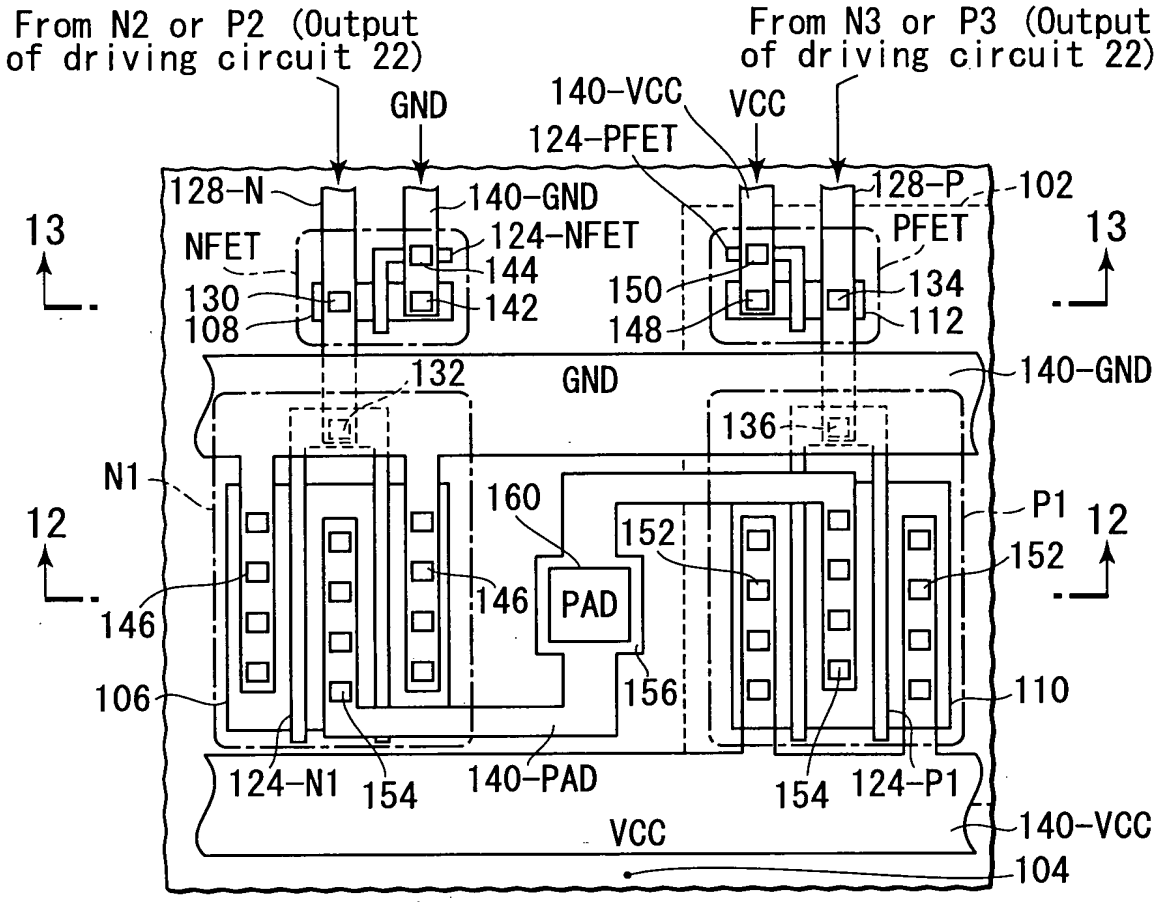

From N2 or P2 (Output of driving circuit 22)
From N3 or P3 (Output of driving circuit 22)
GND
140-VCC
VCC
124-PFET
128-N
140-GND
124-NFET
128-P
102
13
NFET
PFET
144
134
130
142
150
112
108
148
132
GND
140-GND
136
N1
160
P1
12
152
152
146
PAD
146
106
156
110
124-N1
154
140-PAD
154
124-P1
VCC
140-VCC
104

FIG. 11

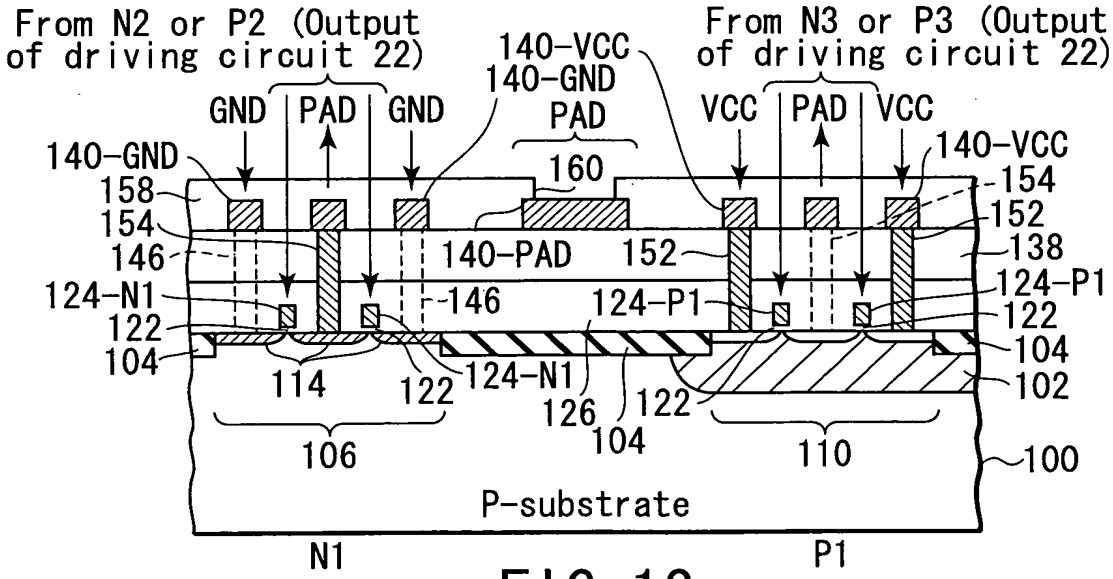

From N2 or P2 (Output of driving circuit 22)
From N3 or P3 (Output of driving circuit 22)
140-VCC
140-GND
GND
PAD
GND
PAD
VCC
PAD
VCC
140-GND
160
140-VCC
158
154
154
152
146
140-PAD
152
138
124-N1
146
124-P1
124-P1
122
122
104
104
114
122
124-N1
126
122
102
104
106
110
100
P-substrate
N1
P1

FIG. 12

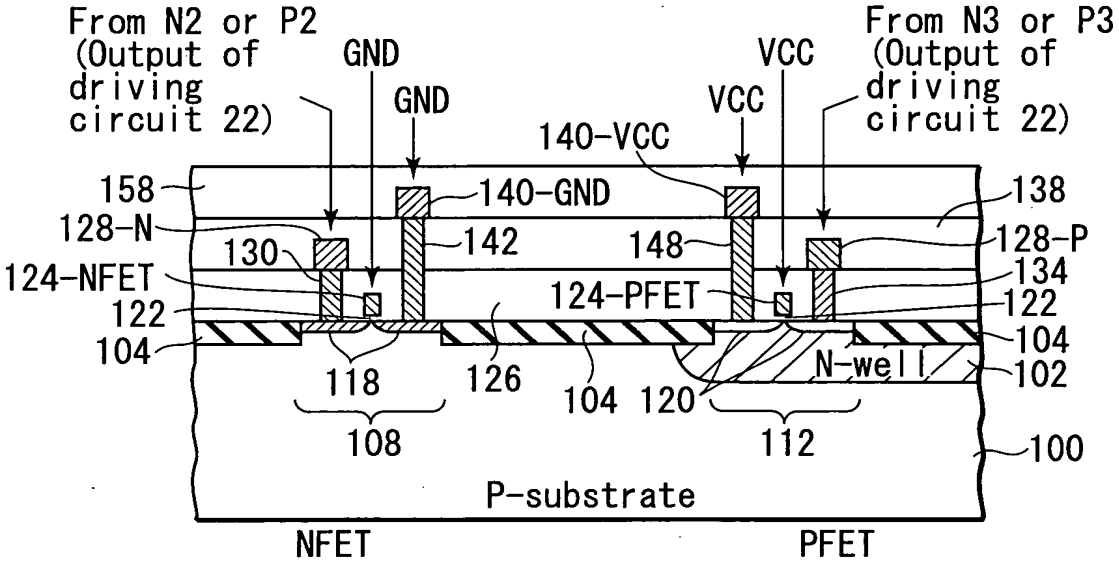

From N2 or P2 (Output of driving circuit 22)
GND
GND
VCC
VCC
From N3 or P3 (Output of driving circuit 22)
140-VCC
158
140-GND
138
128-N
142
148
128-P
130
124-NFET
124-PFET
134
122
122
104
104
N-well
102
118
126
104
120
108
112
100
P-substrate
NFET
PFET

FIG. 13

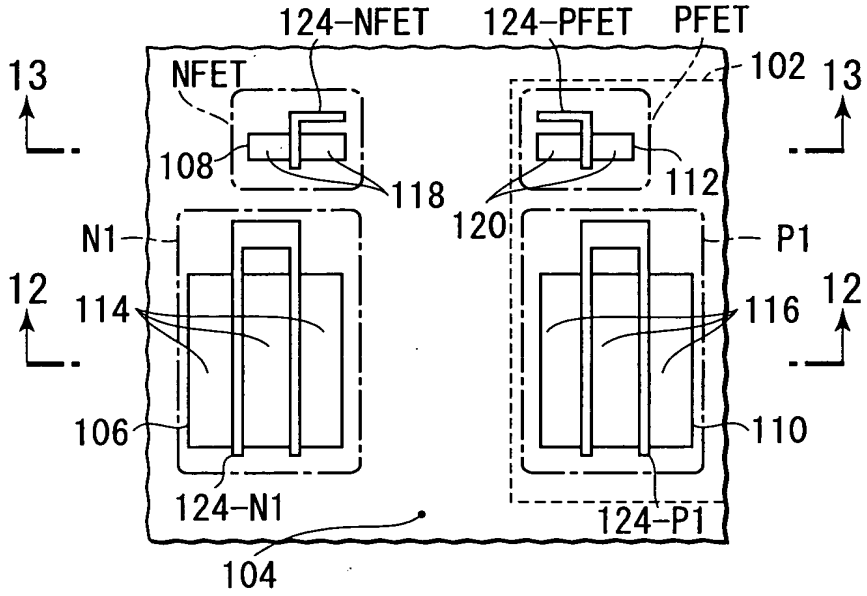

124-NFET
124-PFET
PFET
13
NFET
102
13
108
118
112
120
N1
P1
12
114
116
12
106
110
124-N1
124-P1
104

FIG. 14

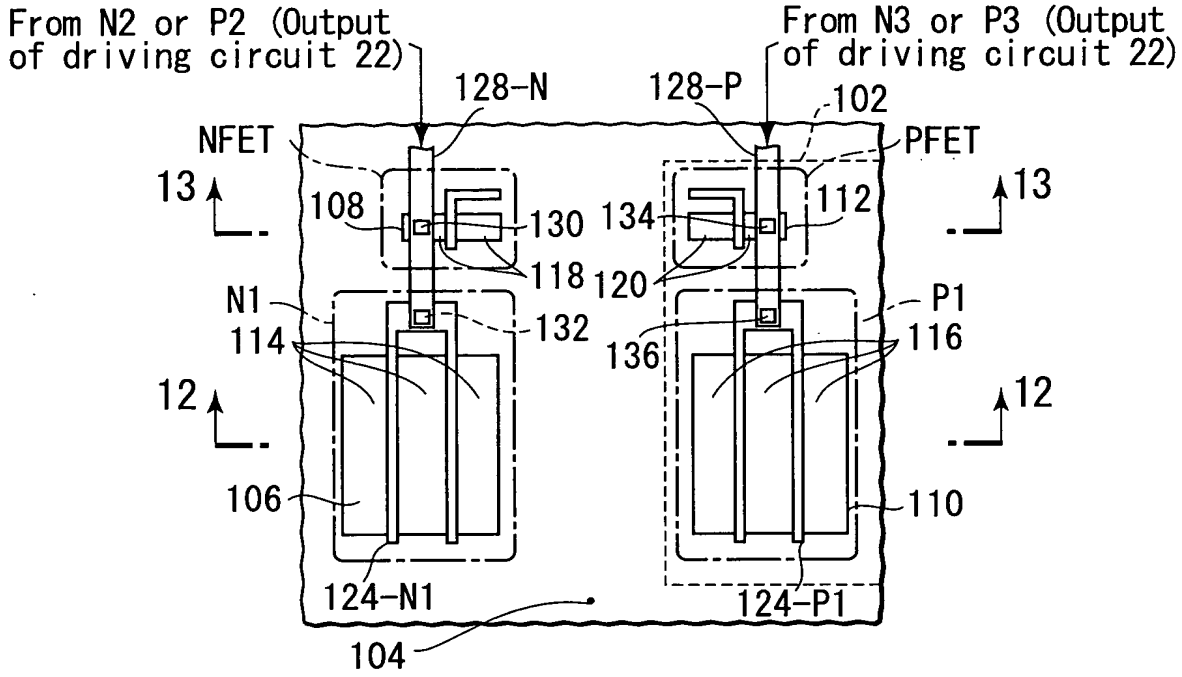

From N2 or P2 (Output of driving circuit 22)
From N3 or P3 (Output of driving circuit 22)
128-N
128-P
102
NFET
PFET
13
13
108
130
134
112
118
120
N1
P1
132
114
136
116
12
12
106
110
124-N1
124-P1
104

FIG. 15

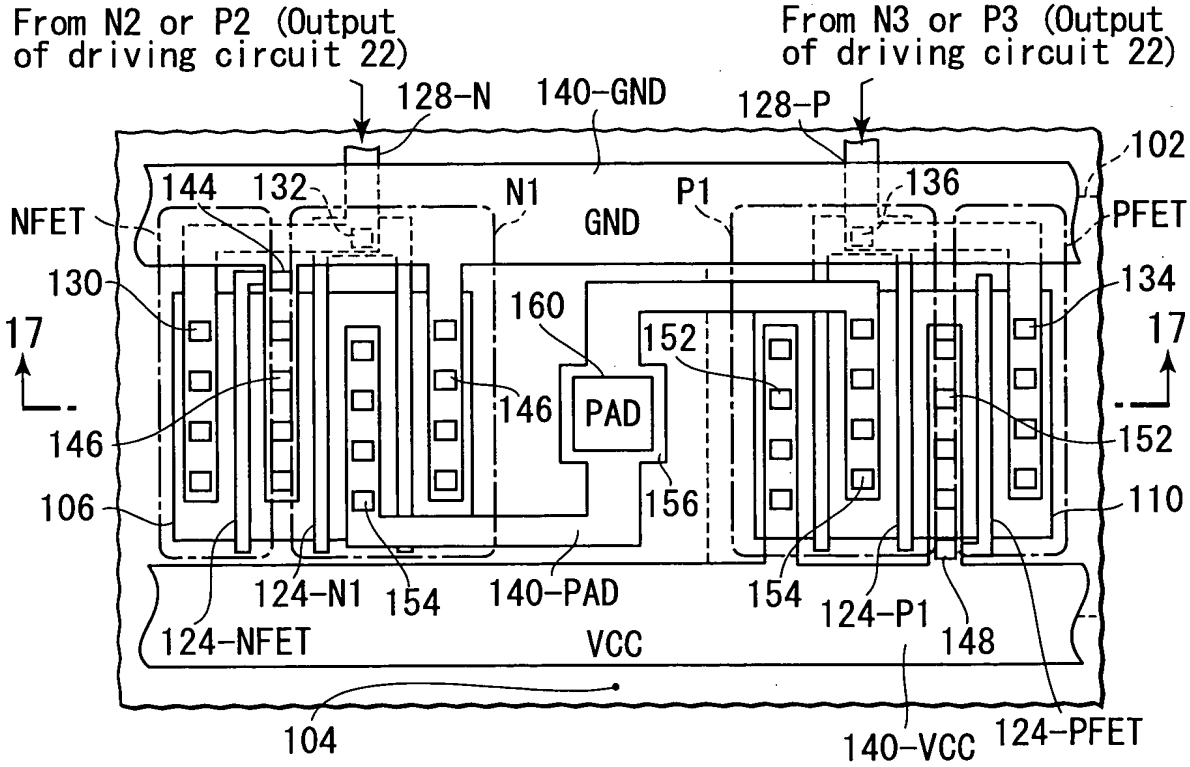

From N2 or P2 (Output of driving circuit 22)
From N3 or P3 (Output of driving circuit 22)
128-N
140-GND
128-P
102
144
132
N1
GND
P1
136
NFET
PFET
130
160
134
17
152
17
146
PAD
146
152
106
156
110
124-N1
154
140-PAD
154
124-P1
148
124-NFET
VCC
104
140-VCC
124-PFET

FIG. 16

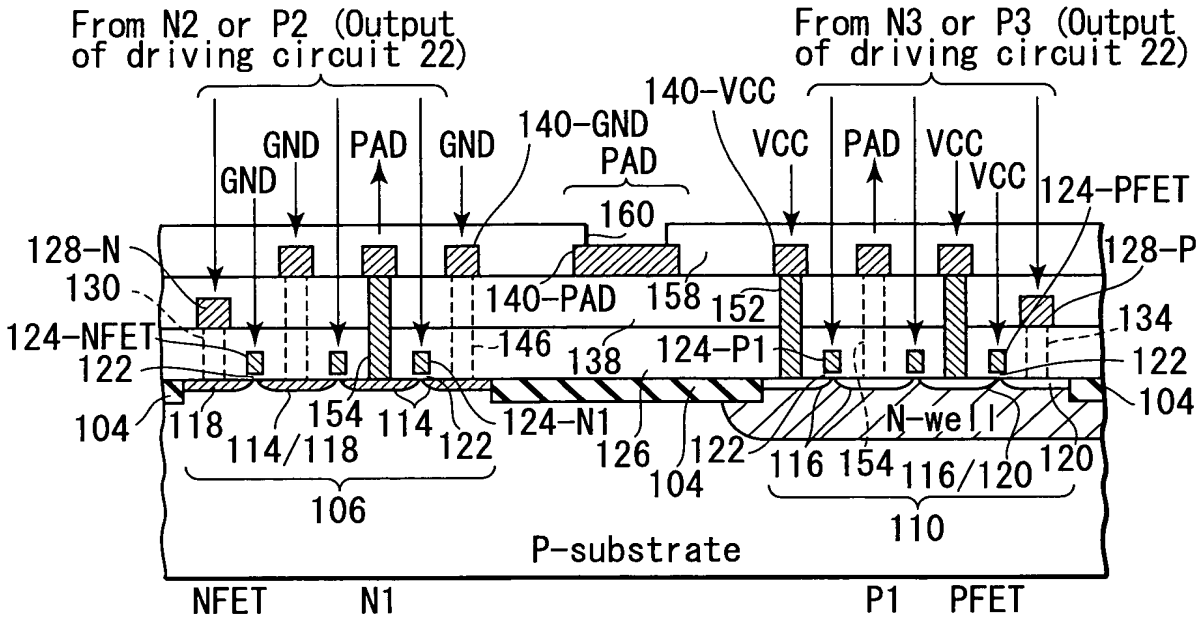


FIG. 17

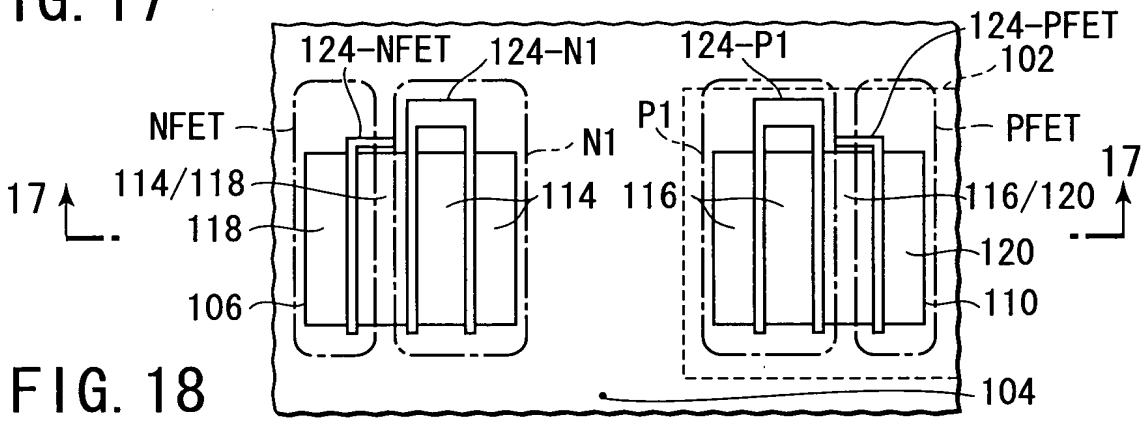


FIG. 18

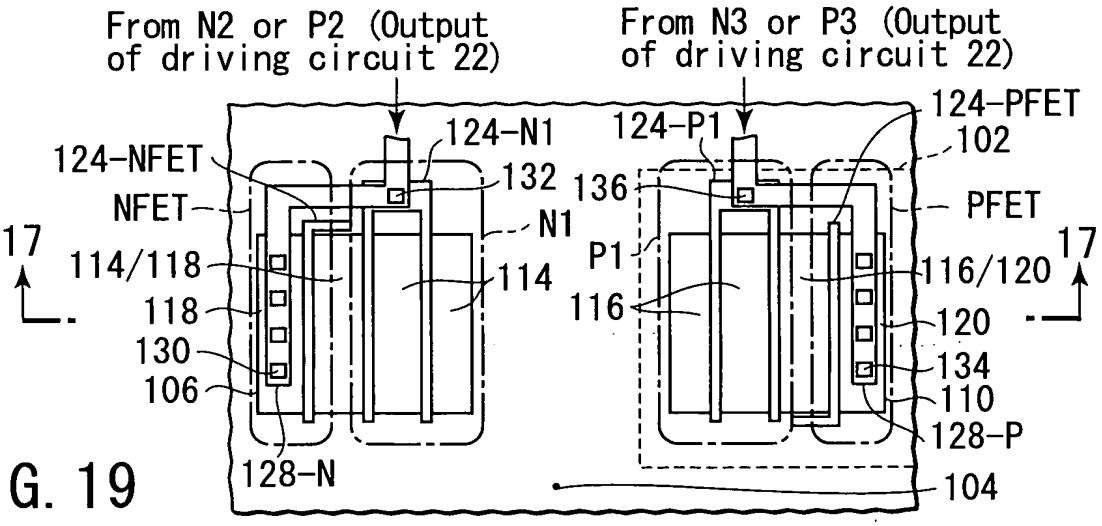


FIG. 19

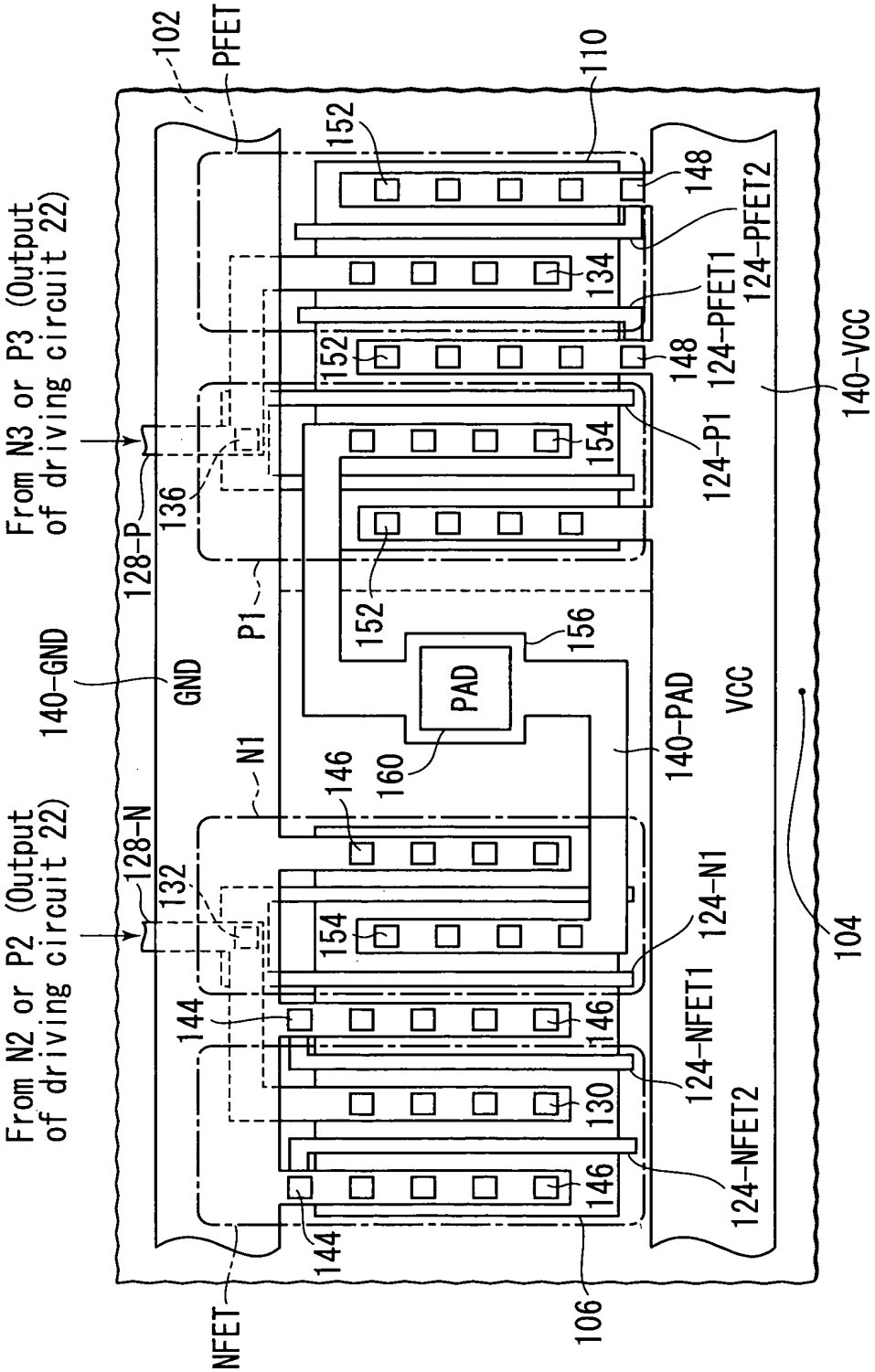

102
PFET
110
152
148
124-PFET2
134
124-PFET1
148
152
124-P1
140-VCC
From N3 or P3 (Output of driving circuit 22)
128-P
136
154
152
P1
156
PAD
160
140-GND
GND
N1
146
140-PAD
VCC
From N2 or P2 (Output of driving circuit 22)
128-N
132
154
124-N1
104
144
146
124-NFET1
130
124-NFET2
146
144
NFET
106

FIG. 20

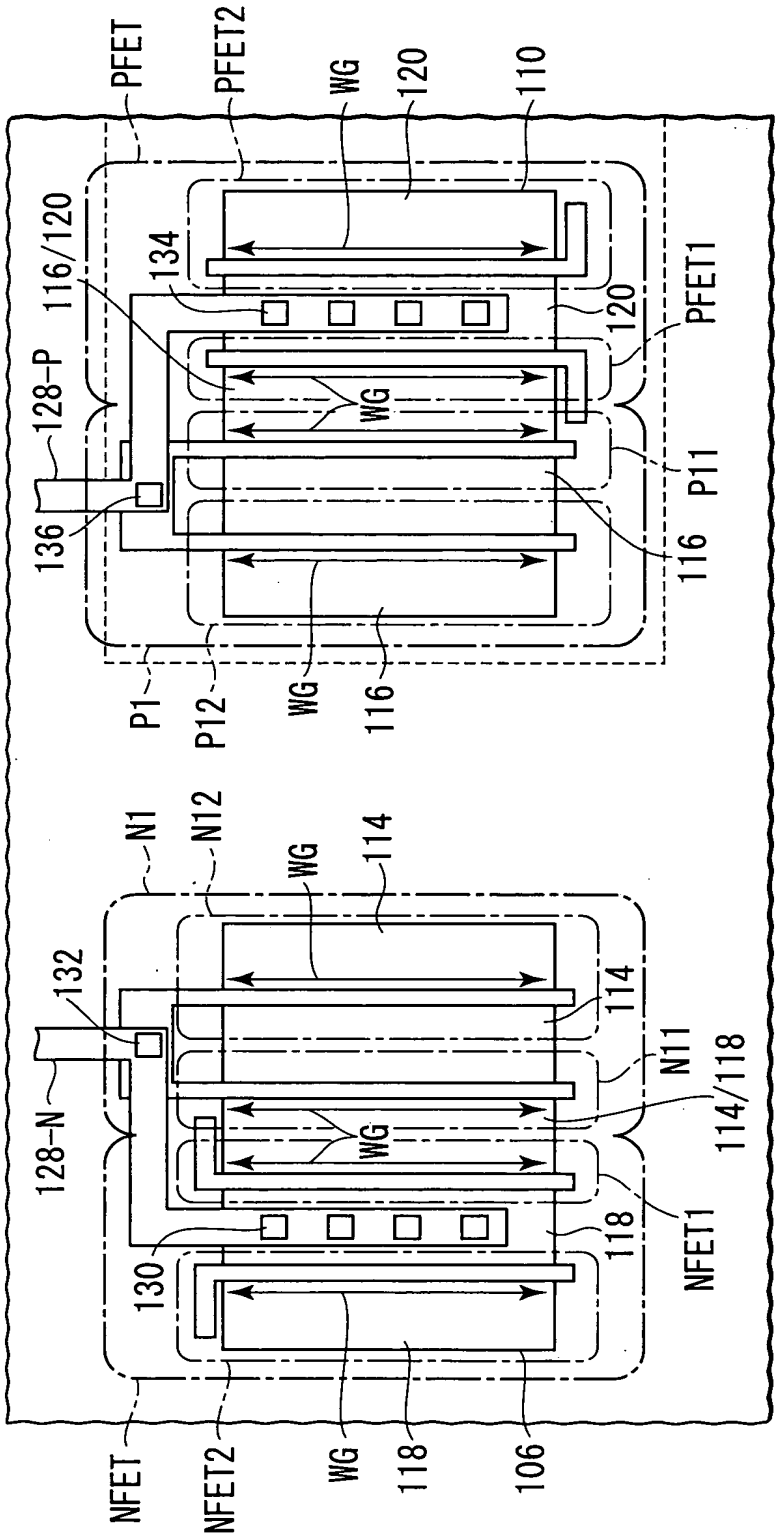

PFET
PFET2
WG
120
110
116/120
134
128-P
136
WG
120
PFET1
P11
116
P1
P12
WG
116
N1
N12
WG
114
132
128-N
WG
114
N11
114/118
130
118
NFET1
NFET
NFET2
WG
118
106

FIG. 21

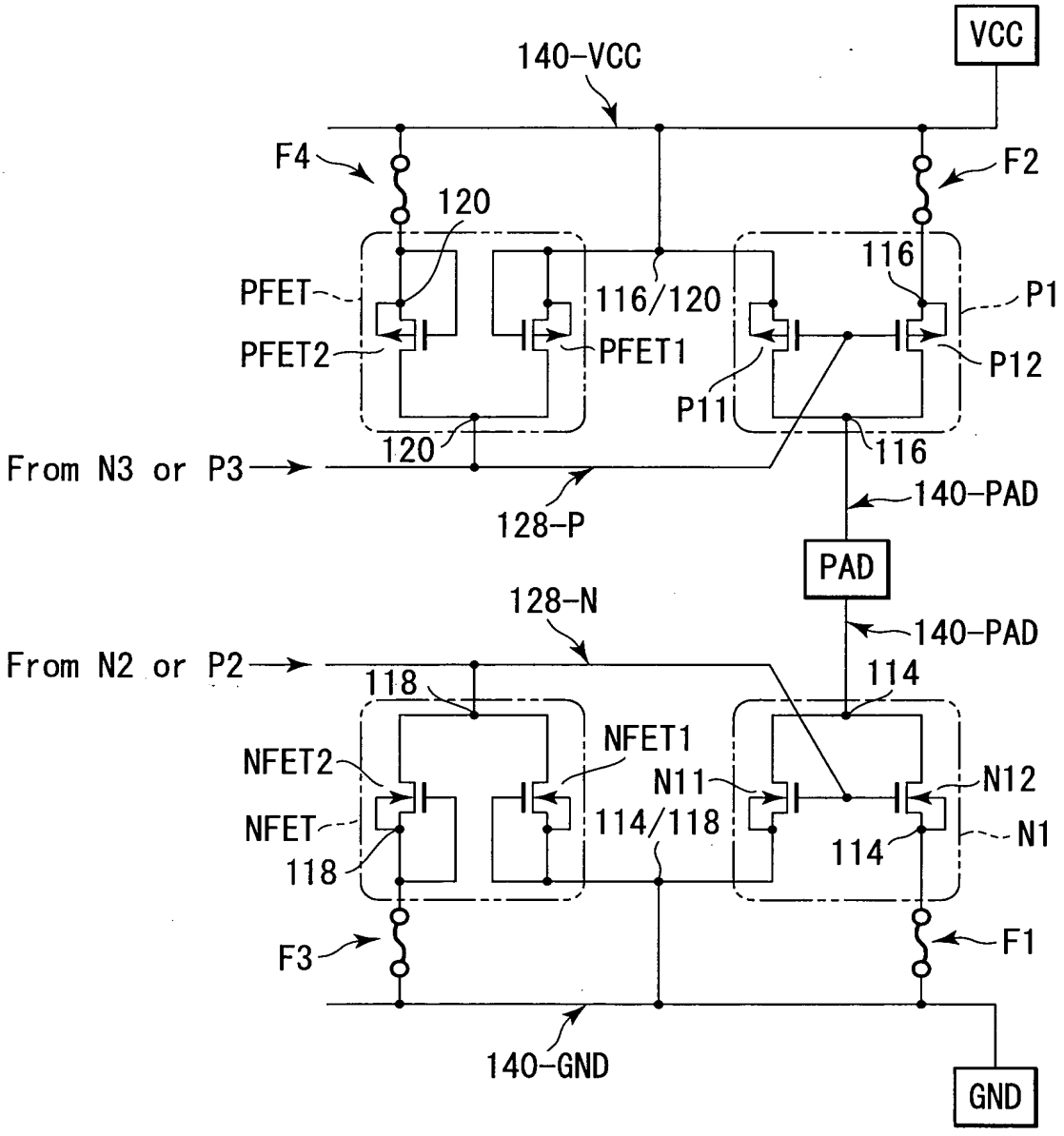

VCC
140-VCC
F4
F2
120
116
PFET
116/120
P1
PFET2
PFET1
P12
P11
120
116
From N3 or P3
140-PAD
128-P
PAD
128-N
140-PAD
From N2 or P2
118
114
NFET1
NFET2
N11
N12
NFET
114/118
N1
118
114
F3
F1
140-GND
GND

FIG. 22

Fuse				Protect ability		Drive ability	
F4	F3	F2	F1	PFET	NFET	P1	N1
0	0	0	0	2WG	2WG	2WG	2WG
0	0	0	1	2WG	2WG	2WG	WG
0	0	1	0	2WG	2WG	WG	2WG
0	0	1	1	2WG	2WG	WG	WG
0	1	0	0	2WG	WG	2WG	2WG
0	1	0	1	2WG	WG	2WG	WG
0	1	1	0	2WG	WG	WG	2WG
0	1	1	1	2WG	WG	WG	WG
1	0	0	0	WG	2WG	2WG	2WG
1	0	0	1	WG	2WG	2WG	WG
1	0	1	0	WG	2WG	WG	2WG
1	0	1	1	WG	2WG	WG	WG
1	1	0	0	WG	WG	2WG	2WG
1	1	0	1	WG	WG	2WG	WG
1	1	1	0	WG	WG	WG	2WG
1	1	1	1	WG	WG	WG	WG

0:Connect
1:Disconnect

FIG. 23

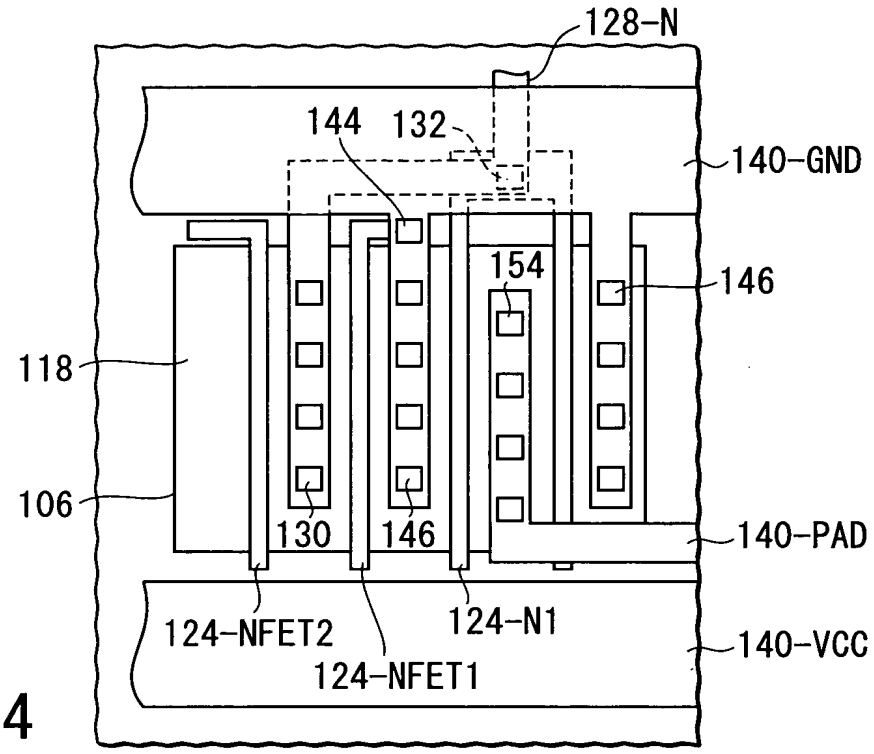

128-N
144
132
140-GND
154
146
118
106
130
146
140-PAD
124-NFET2
124-N1
140-VCC
124-NFET1

FIG. 24

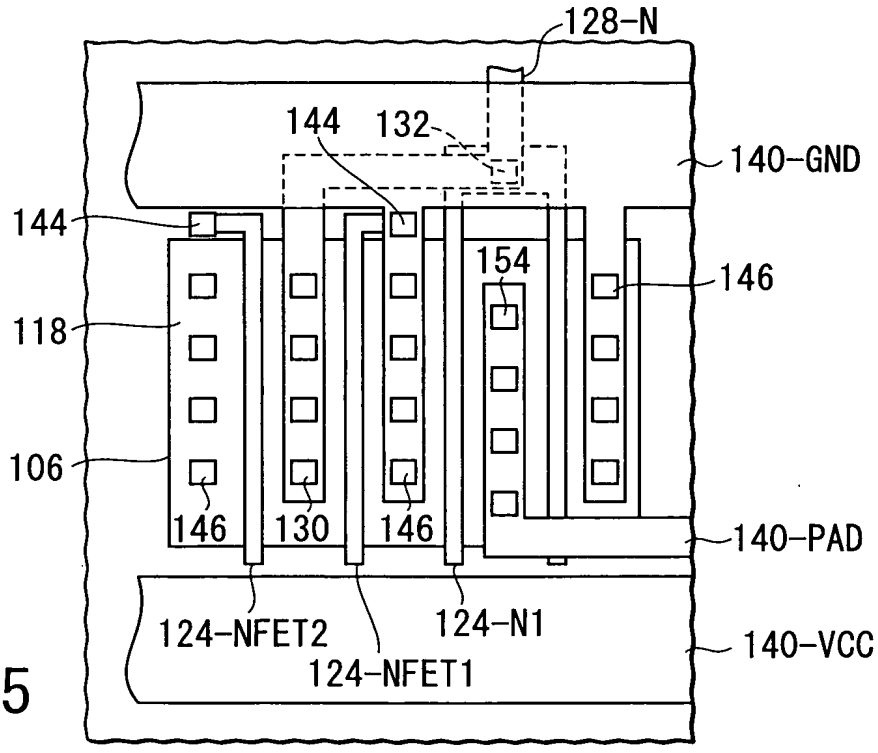

128-N
144
132
140-GND
144
154
146
118
106
146
130
146
140-PAD
124-NFET2
124-N1
140-VCC
124-NFET1

FIG. 25

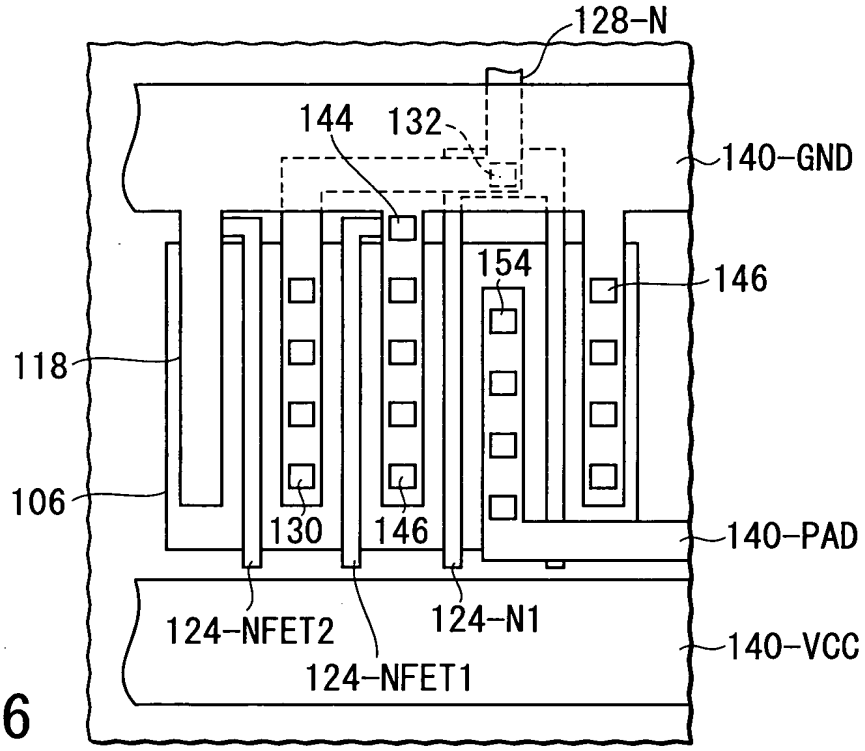

128-N
144
132
140-GND
154
146
118
106
130
146
140-PAD
124-NFET2
124-N1
140-VCC
124-NFET1

FIG. 26

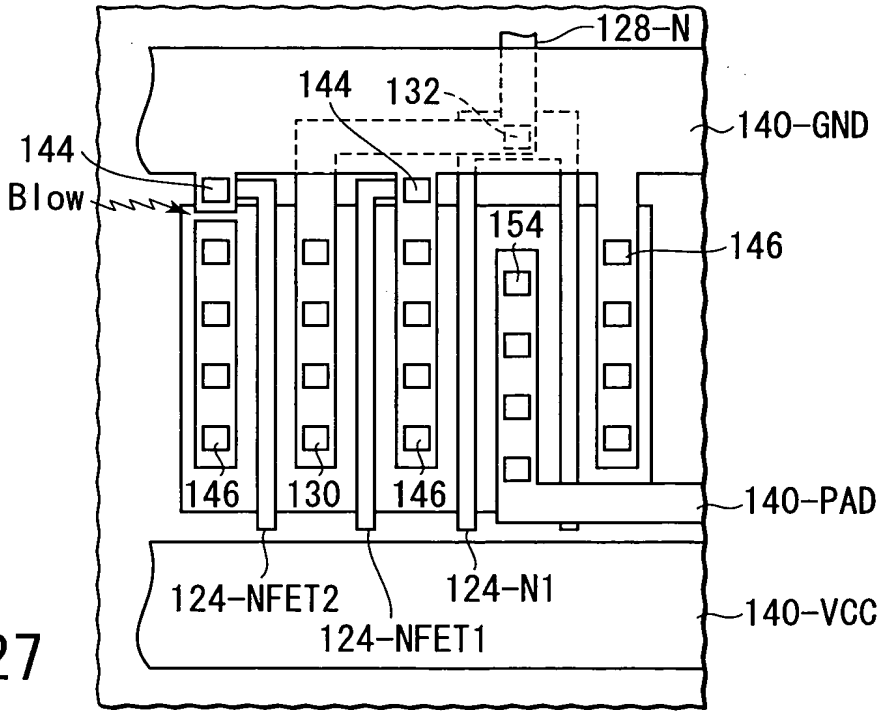

128-N
144
132
140-GND
144
Blow
154
146
146
130
146
140-PAD
124-NFET2
124-N1
140-VCC
124-NFET1

FIG. 27

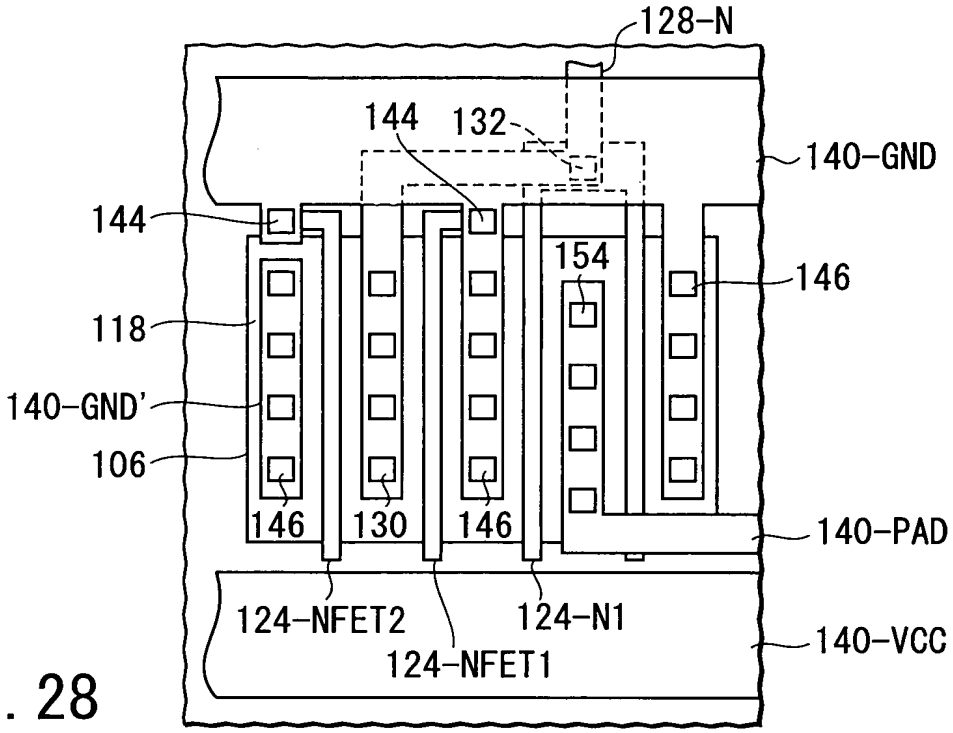

128-N
144
132
140-GND
144
154
146
118
140-GND'
106
146
130
146
140-PAD
124-NFET2
124-N1
140-VCC
124-NFET1

FIG. 28

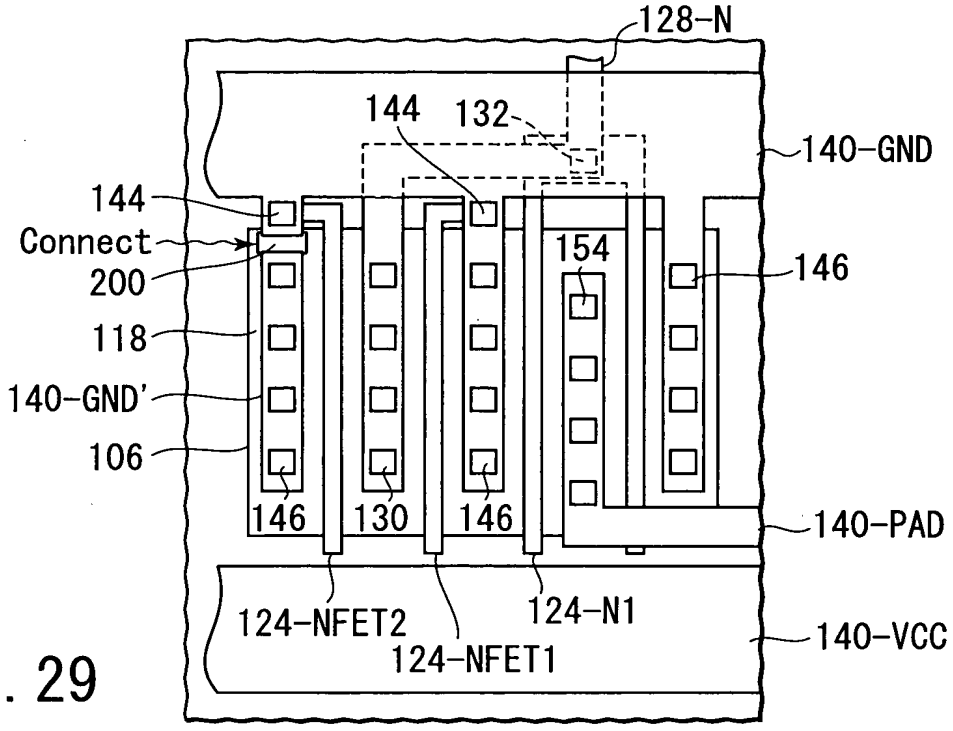

128-N
144
132
140-GND
144
Connect
200
154
146
118
140-GND'
106
146
130
146
140-PAD
124-NFET2
124-N1
140-VCC
124-NFET1

FIG. 29

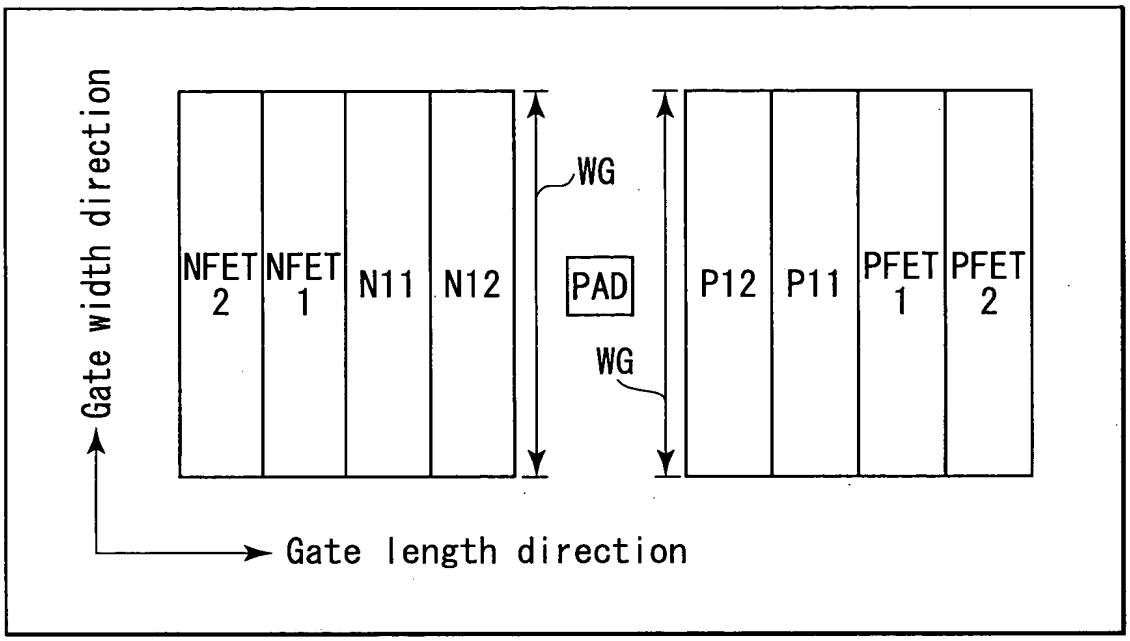

Gate width direction
NFET 2
NFET 1
N11
N12
WG
PAD
WG
P12
P11
PFET 1
PFET 2
Gate length direction

FIG. 30

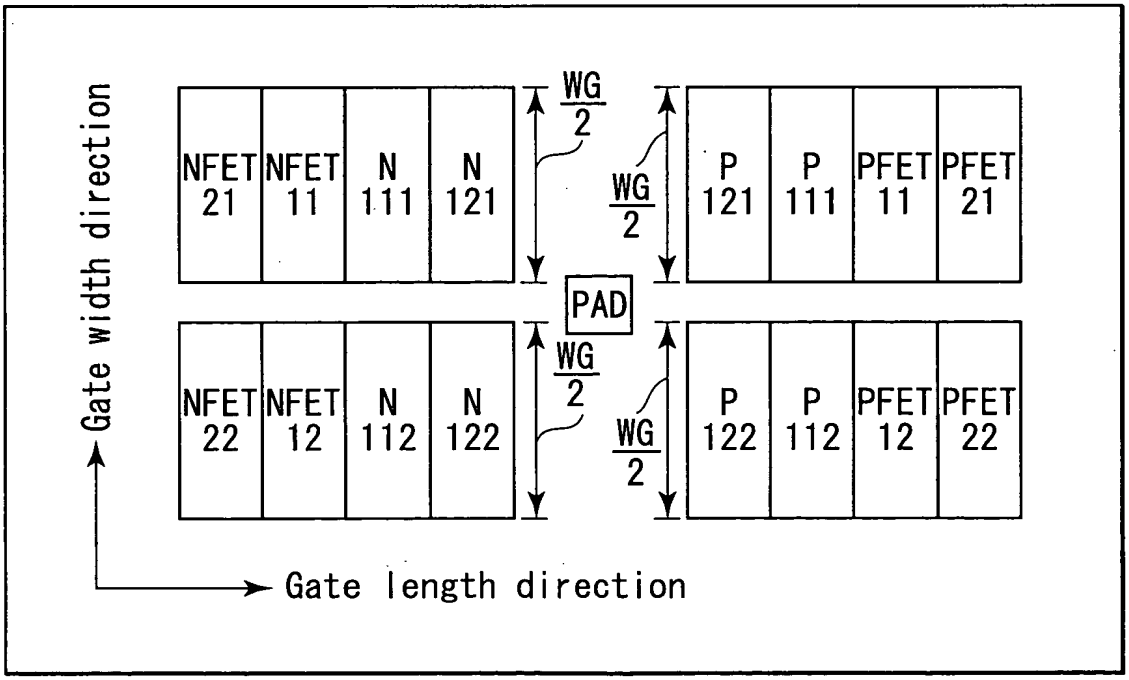

Gate width direction
NFET 21
NFET 11
N 111
N 121
WG 2
WG 2
P 121
P 111
PFET 11
PFET 21
PAD
NFET 22
NFET 12
N 112
N 122
WG 2
WG 2
P 122
P 112
PFET 12
PFET 22
Gate length direction

FIG. 31

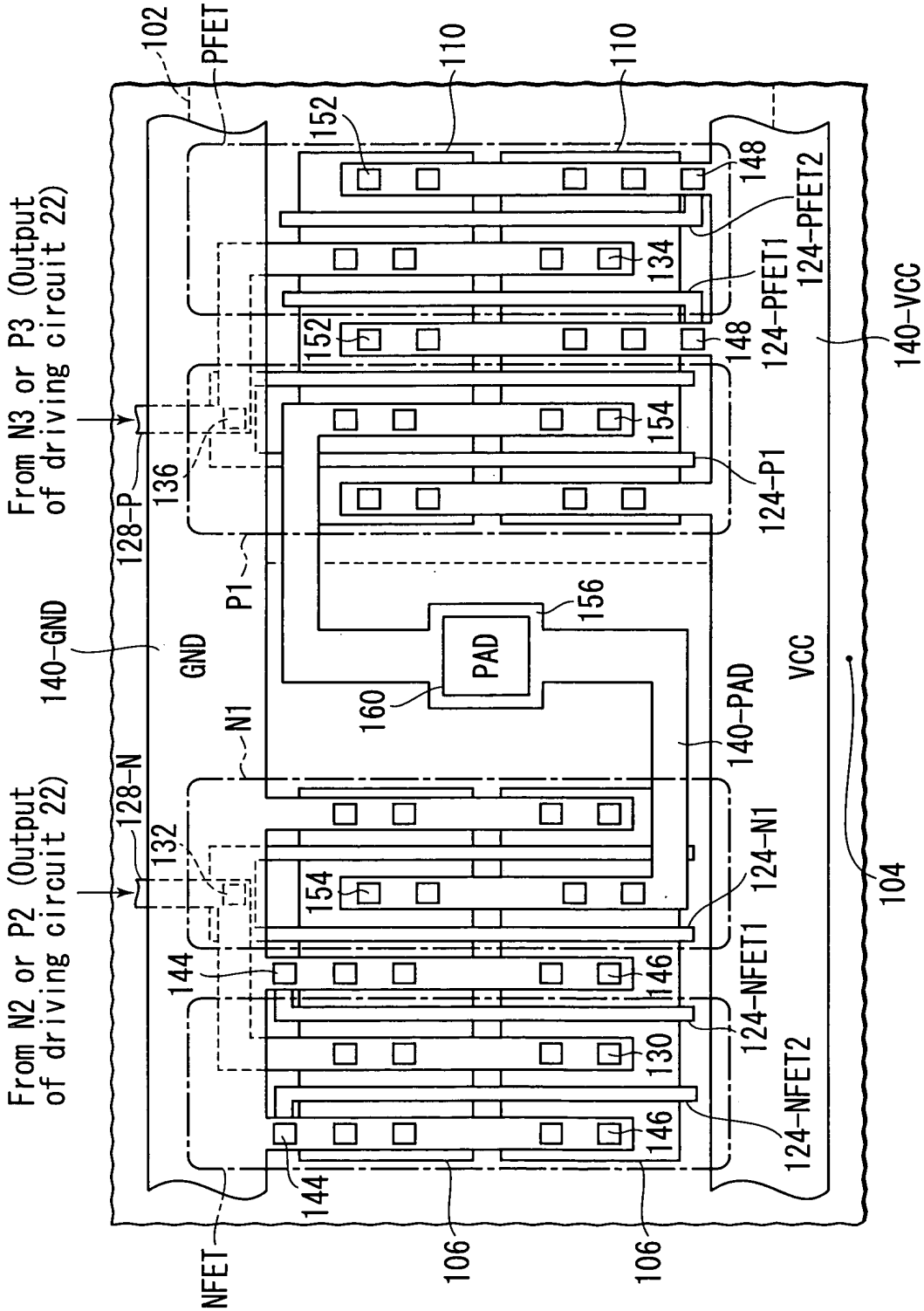

102
PFET
110
110
152
148
124-PFET2
134
124-PFET1
140-VCC
From N3 or P3 (Output of driving circuit 22)
128-P
136
154
124-P1
P1
156
140-GND
GND
PAD
160
N1
140-PAD
VCC
128-N
From N2 or P2 (Output of driving circuit 22)
132
154
124-N1
144
146
124-NFET1
130
124-NFET2
104
NFET
106
106

FIG. 32

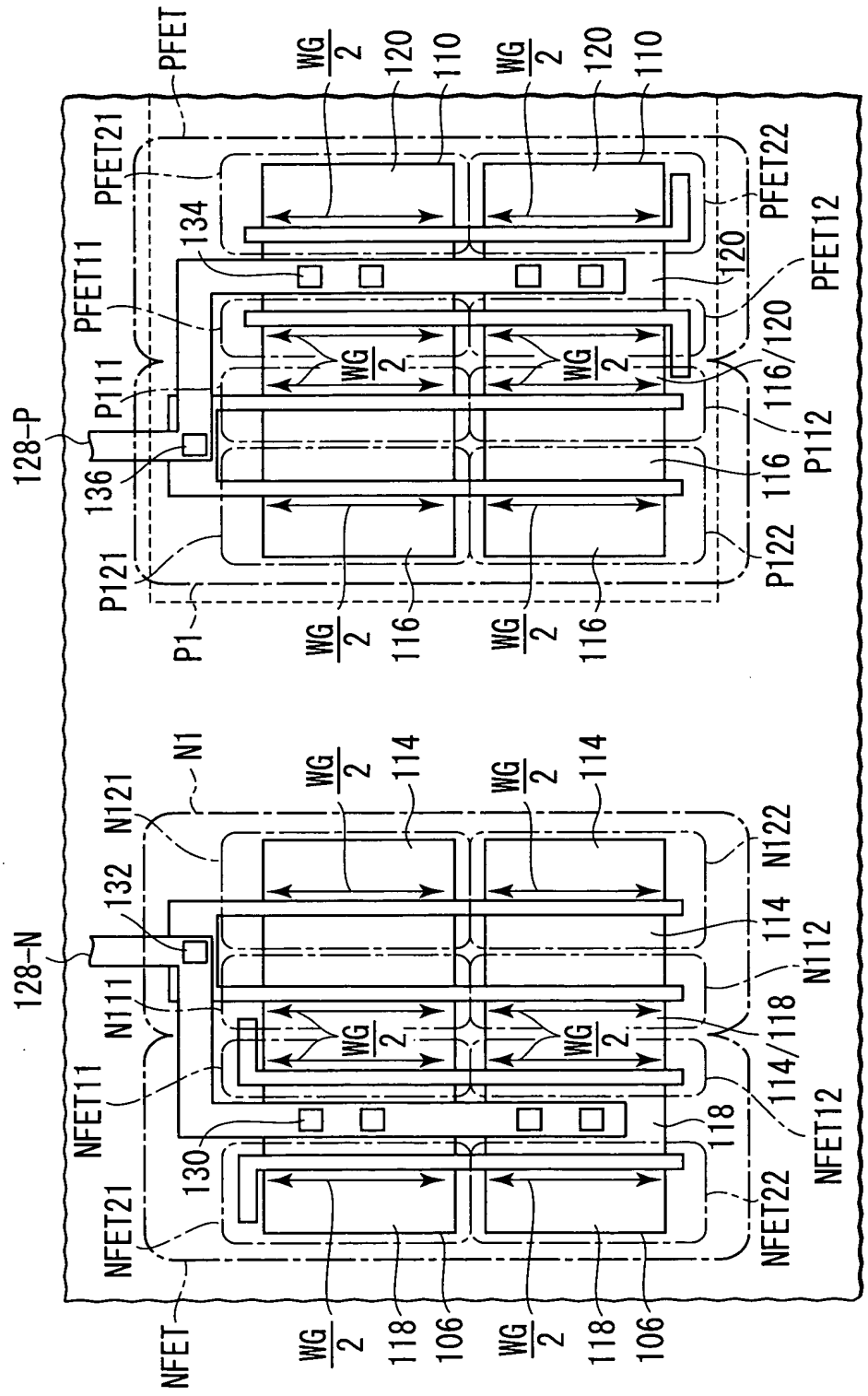

PFET
PFET21
PFET11
PFET22
PFET12
134
120
110
WG/2
128-P
136
P111
P121
P112
P122
116/120
116
P1
N1
N121
N122
N111
N112
NFET11
NFET12
NFET21
NFET22
132
128-N
114
114/118
118
130
106
NFET

FIG. 33

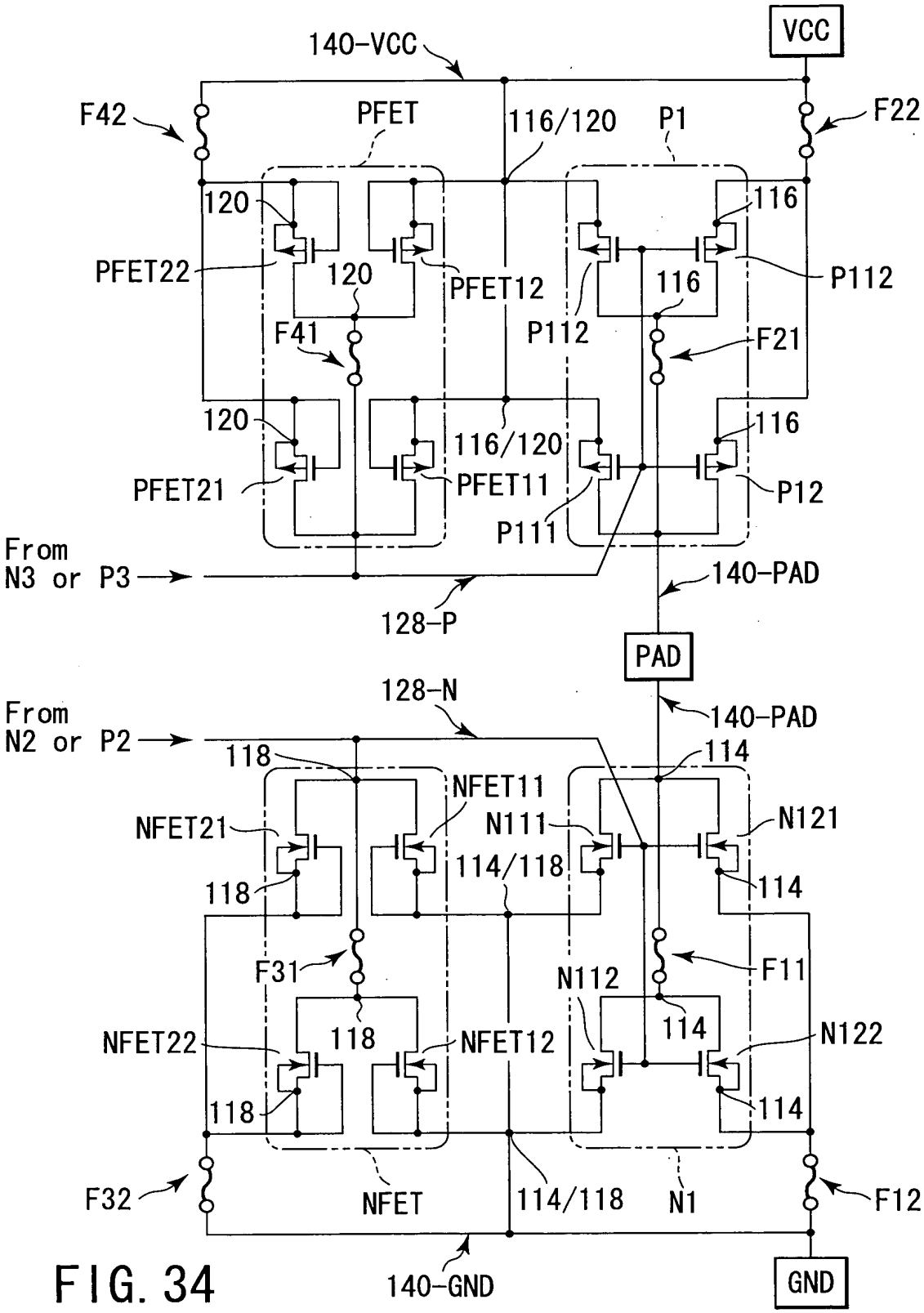

VCC
140-VCC
F42
PFET
116/120
P1
F22
120
116
PFET22
120
PFET12
116
P112
P112
F41
F21
120
116
116/120
PFET21
PFET11
P12
P111
From
N3 or P3
140-PAD
128-P
PAD
128-N
From
N2 or P2
140-PAD
118
114
NFET11
NFET21
N111
N121
114/118
118
114
F31
F11
N112
NFET22
118
NFET12
114
N122
118
114
F32
NFET
114/118
N1
F12
140-GND
GND

FIG. 34

Fuse								Protect ability		Drive ability	
F42	F41	F32	F31	F22	F21	F12	F11	PFET	NFET	P1	N1
0	0	0	0	0	0	0	0	2WG	2WG	2WG	2WG
0	0	0	0	0	0	0	1	2WG	2WG	2WG	1.5WG
0	0	0	0	0	0	1	0	2WG	2WG	2WG	WG
0	0	0	0	0	0	1	1	2WG	2WG	2WG	0.5WG
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	0	0	0	0	0	2WG	2WG	2WG	2WG
0	0	0	0	0	1	0	0	2WG	2WG	1.5WG	2WG
0	0	0	0	1	0	0	0	2WG	2WG	WG	2WG
0	0	0	0	1	1	0	0	2WG	2WG	0.5WG	2WG
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	0	0	0	0	0	2WG	2WG	2WG	2WG
0	0	0	1	0	0	0	0	2WG	1.5WG	2WG	2WG
0	0	1	0	0	0	0	0	2WG	WG	2WG	2WG
0	0	1	1	0	0	0	0	2WG	0.5WG	2WG	2WG
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	0	0	0	0	0	2WG	2WG	2WG	2WG
0	1	0	0	0	0	0	0	1.5WG	2WG	2WG	2WG
1	0	0	0	0	0	0	0	WG	2WG	2WG	2WG
1	1	0	0	0	0	0	0	0.5WG	2WG	2WG	2WG

0:Connect

1:Disconnect

FIG. 35

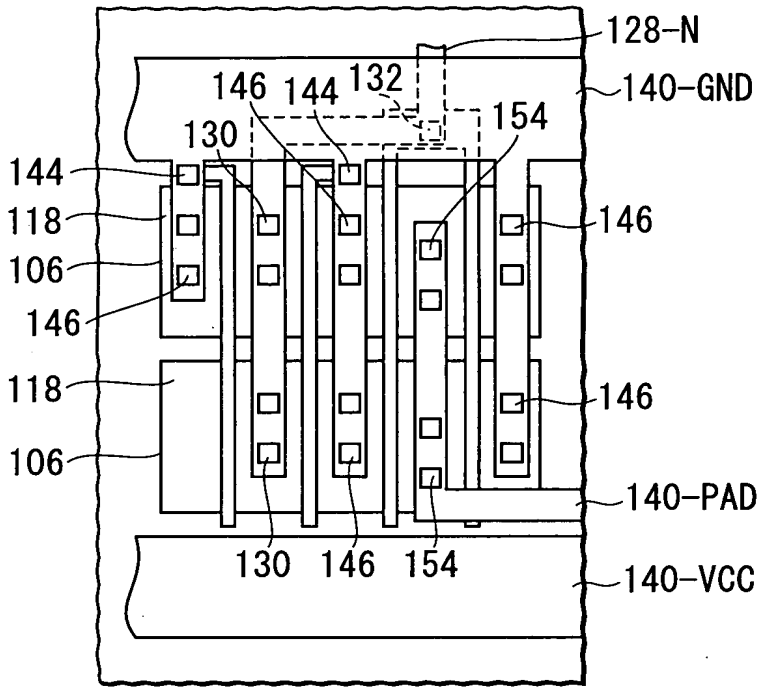

128-N
140-GND
146
144
132
154
130
144
118
106
146
146
118
146
106
140-PAD
130
146
154
140-VCC

FIG. 36

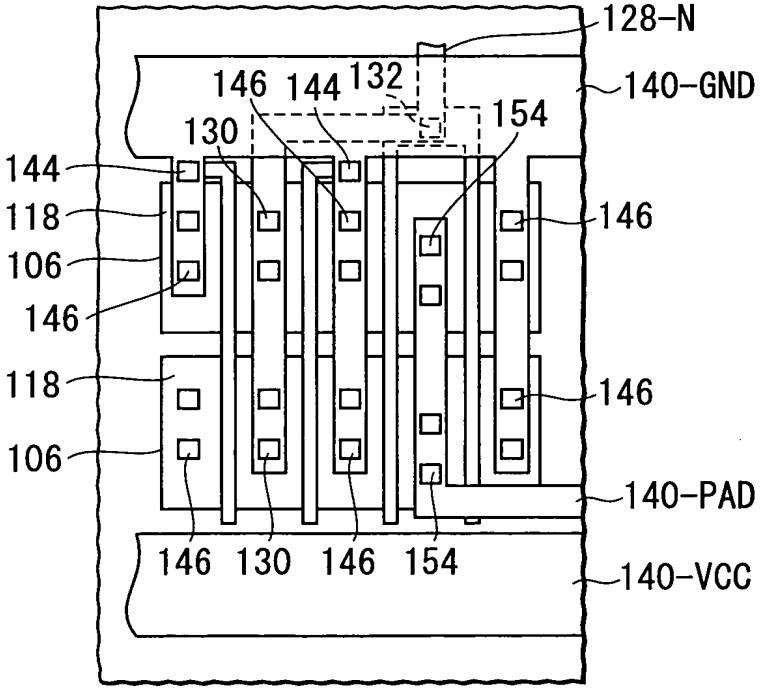

128-N
140-GND
146
144
132
154
130
144
118
106
146
146
118
146
106
140-PAD
146
130
146
154
140-VCC

FIG. 37

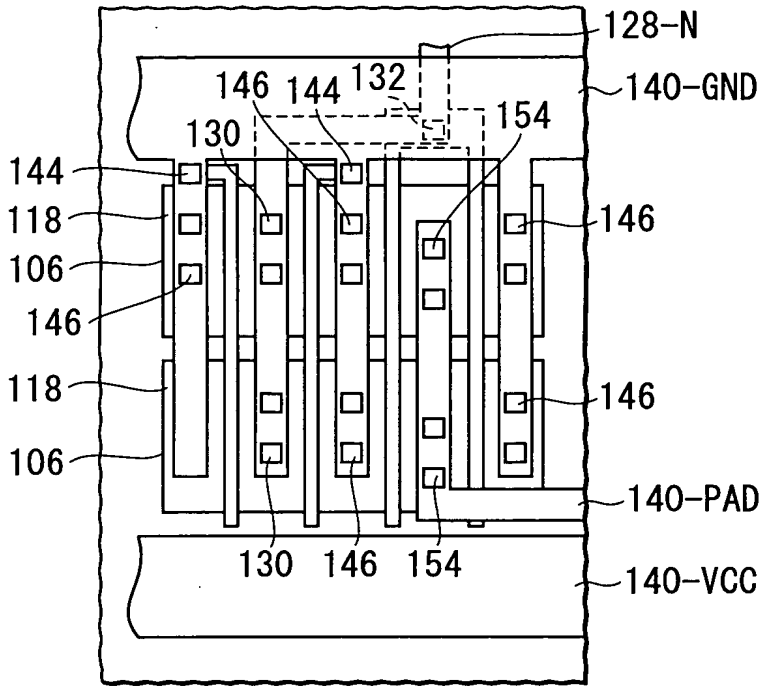

128-N
140-GND
146
144
132
154
130
144
118
106
146
146
118
146
106
140-PAD
130
146
154
140-VCC

FIG. 38

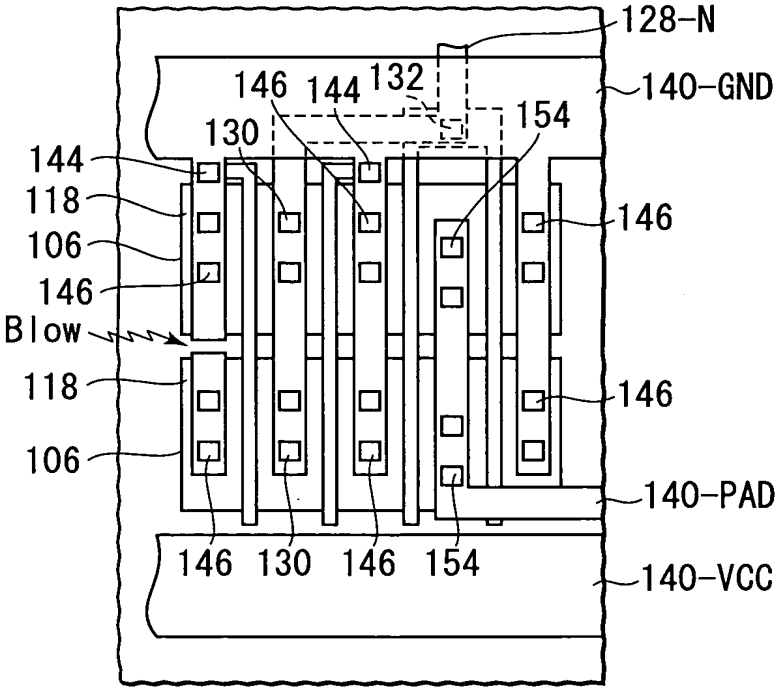

128-N
140-GND
146
144
132
154
130
144
118
106
146
146
Blow
118
146
106
140-PAD
146
130
146
154
140-VCC

FIG. 39

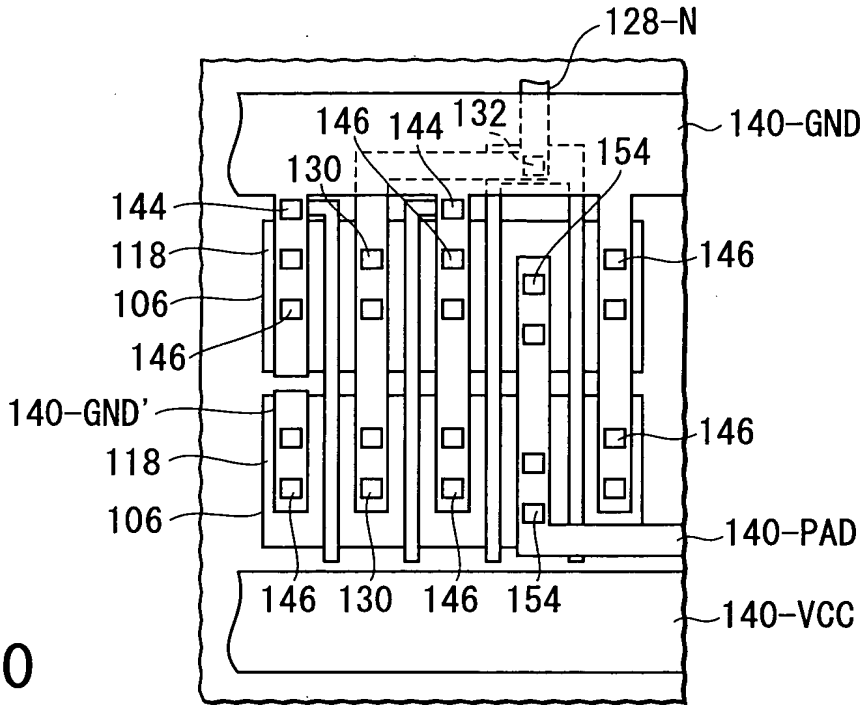

128-N
146
144
132
130
154
140-GND
144
118
106
146
140-GND'
118
106
146
146
140-PAD
146
130
146
154
140-VCC

FIG. 40

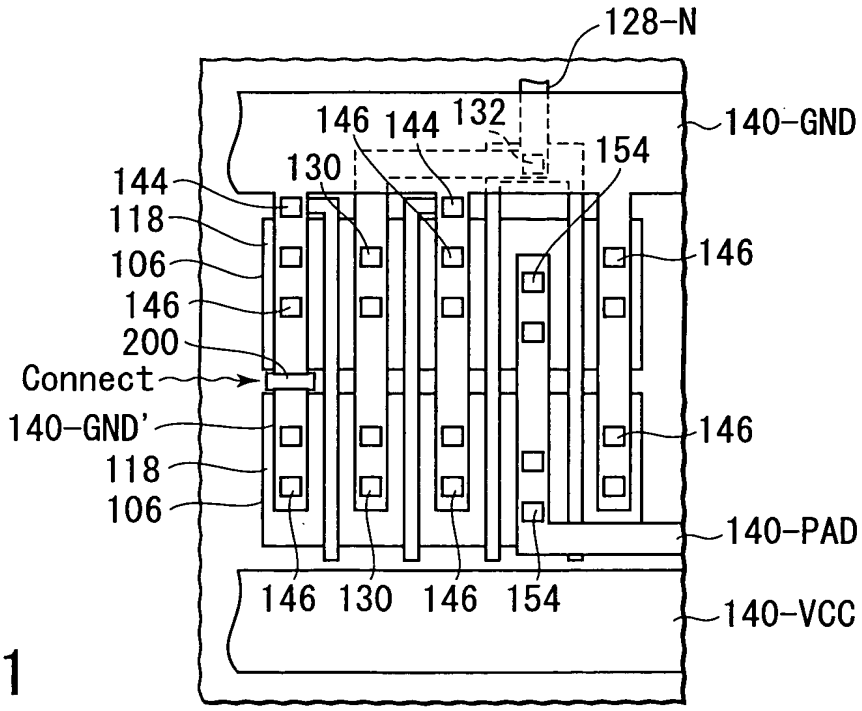

128-N
146
144
132
130
154
140-GND
144
118
106
146
200
Connect
140-GND'
118
106
146
146
140-PAD
146
130
146
154
140-VCC

FIG. 41

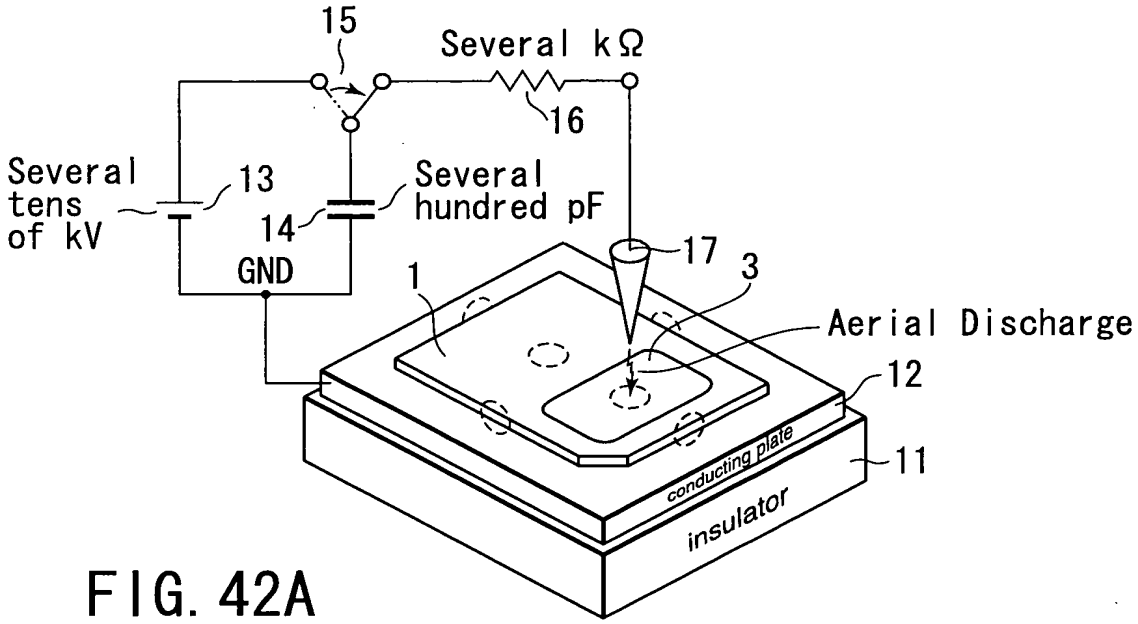


FIG. 42A

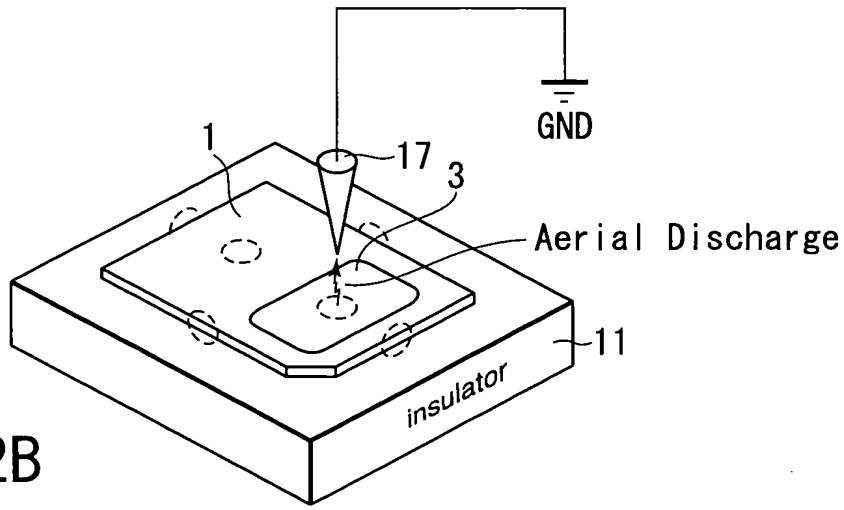


FIG. 42B

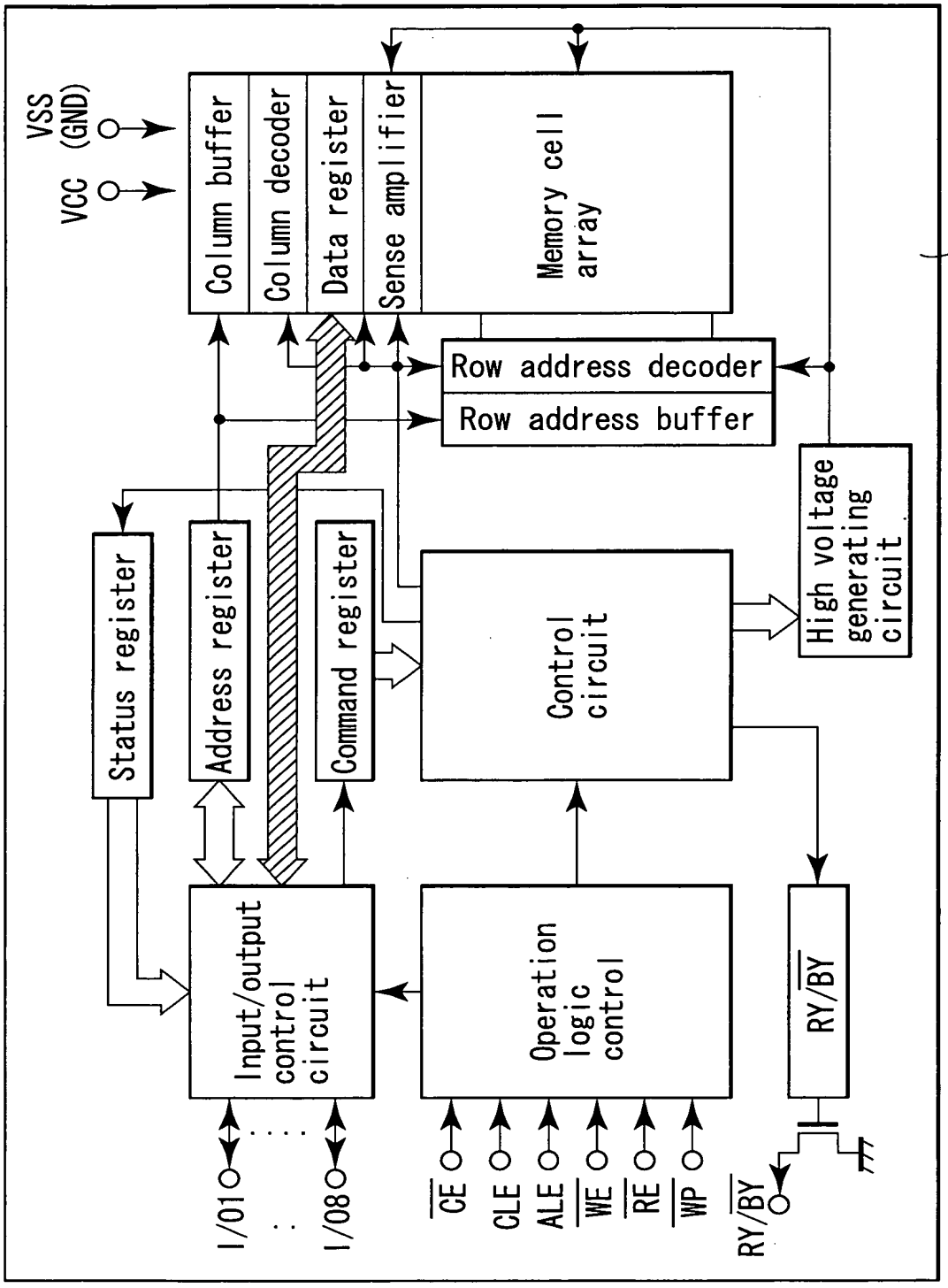

VSS
VCC (GND)
Column buffer
Column decoder
Data register
Sense amplifier
Memory cell array
2
Row address decoder
Row address buffer
High voltage generating circuit
Status register
Address register
Command register
Control circuit
Input/output control circuit
Operation logic control
RY/BY
I/01
I/08
CE
CLE
ALE
WE
RE
WP
RY/BY

FIG. 43A

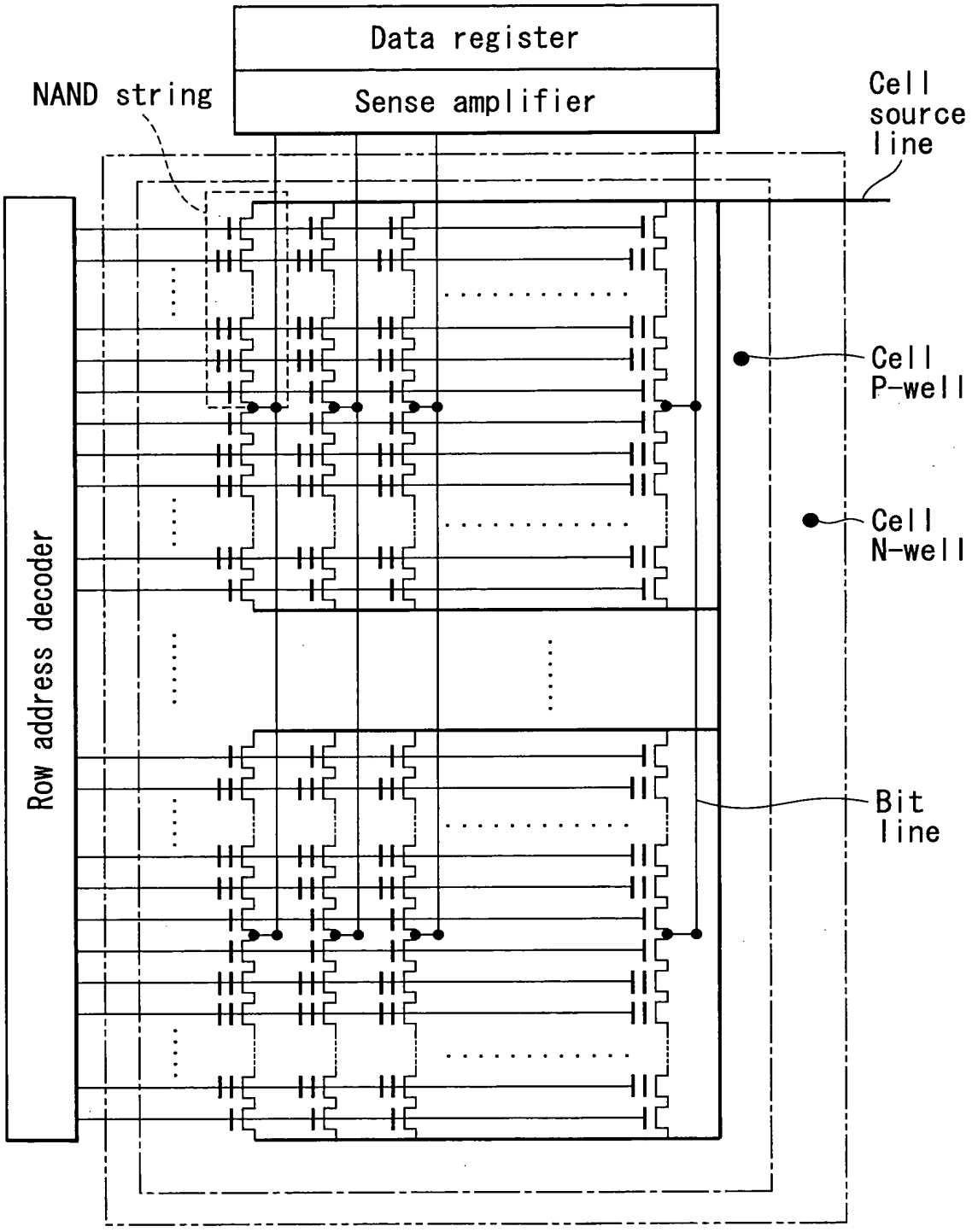

Data register
Sense amplifier
NAND string
Cell source line
Cell P-well
Cell N-well
Bit line
Row address decoder

FIG. 43B

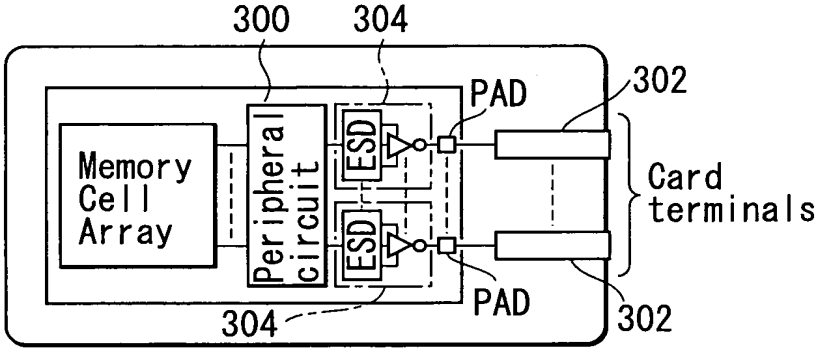


FIG. 44

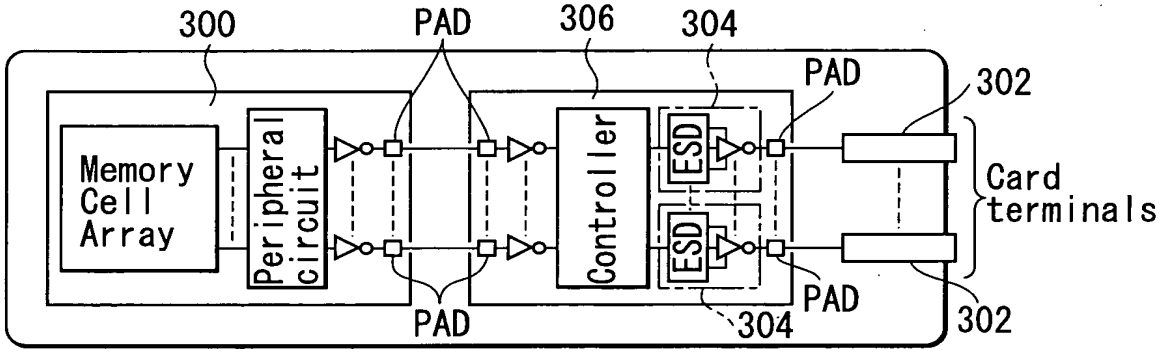


FIG. 45

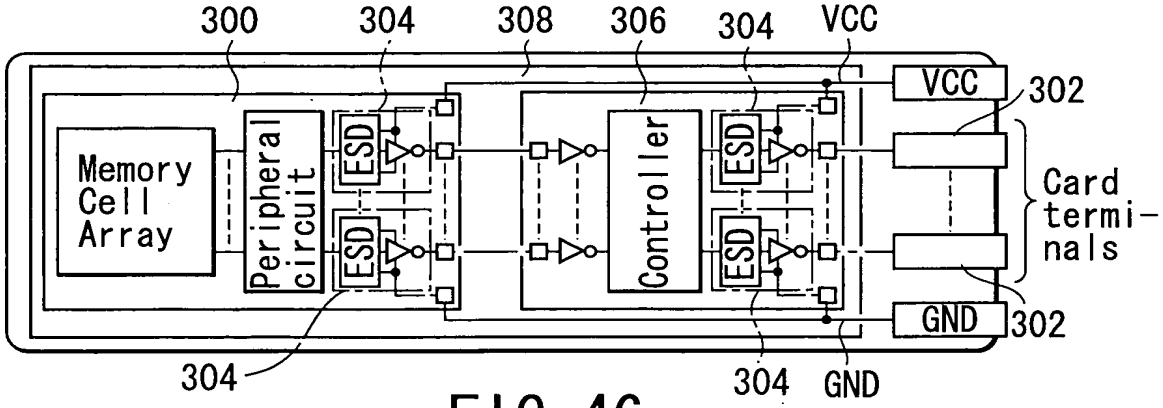


FIG. 46

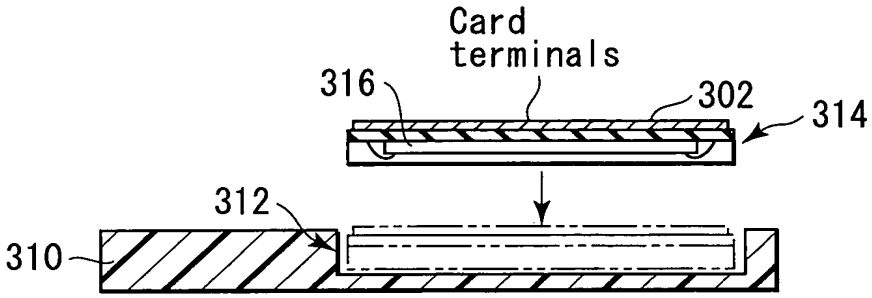


FIG. 47

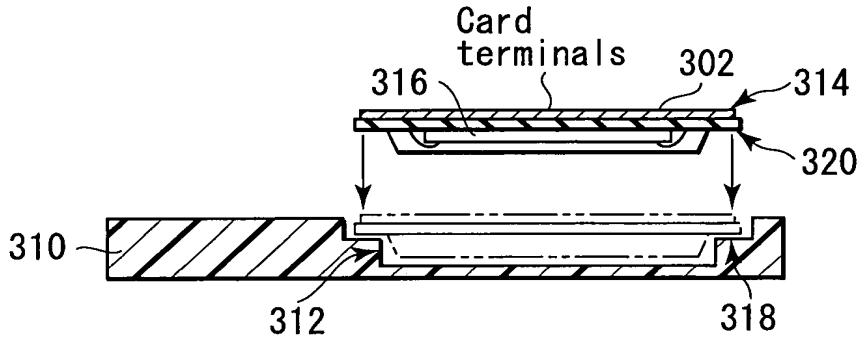


FIG. 48

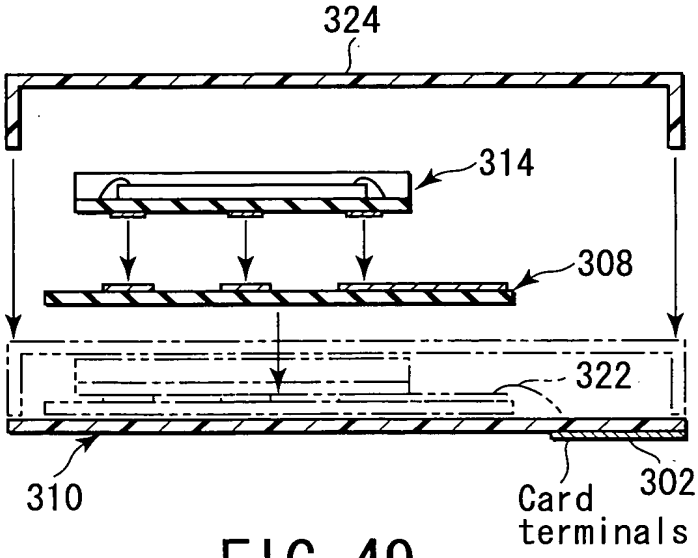


FIG. 49

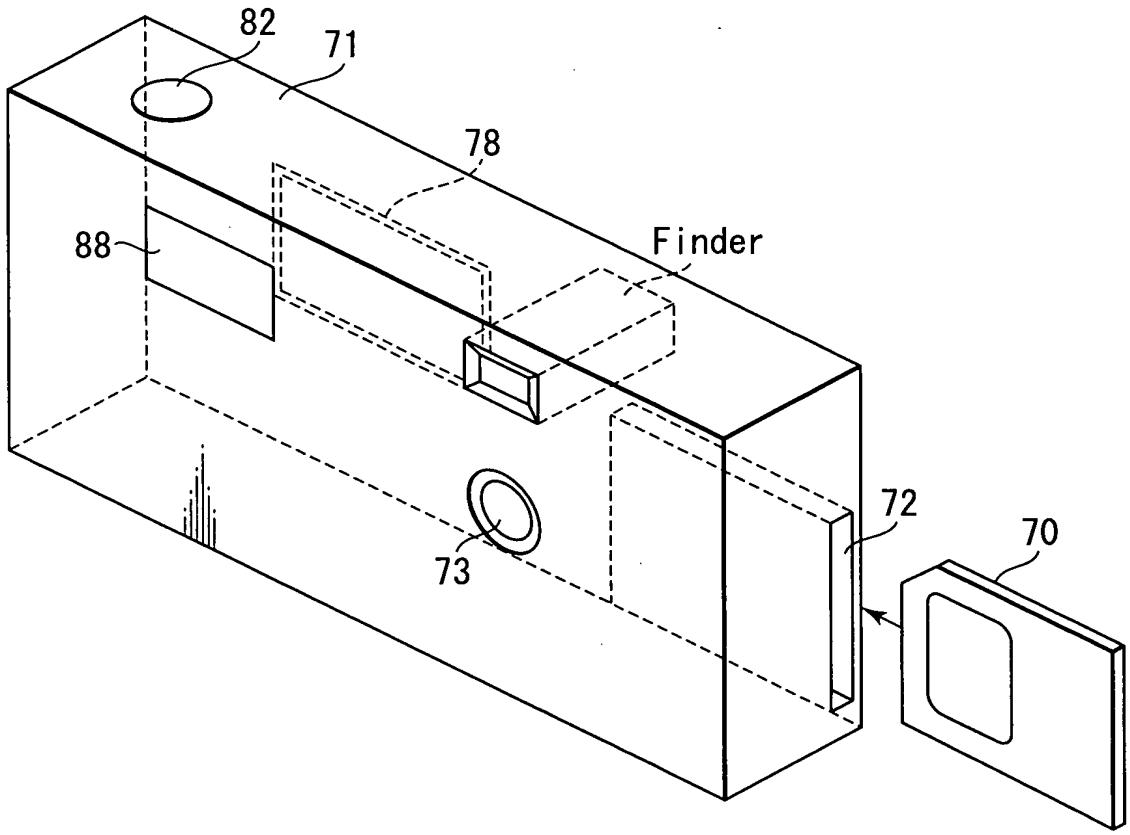


FIG. 50

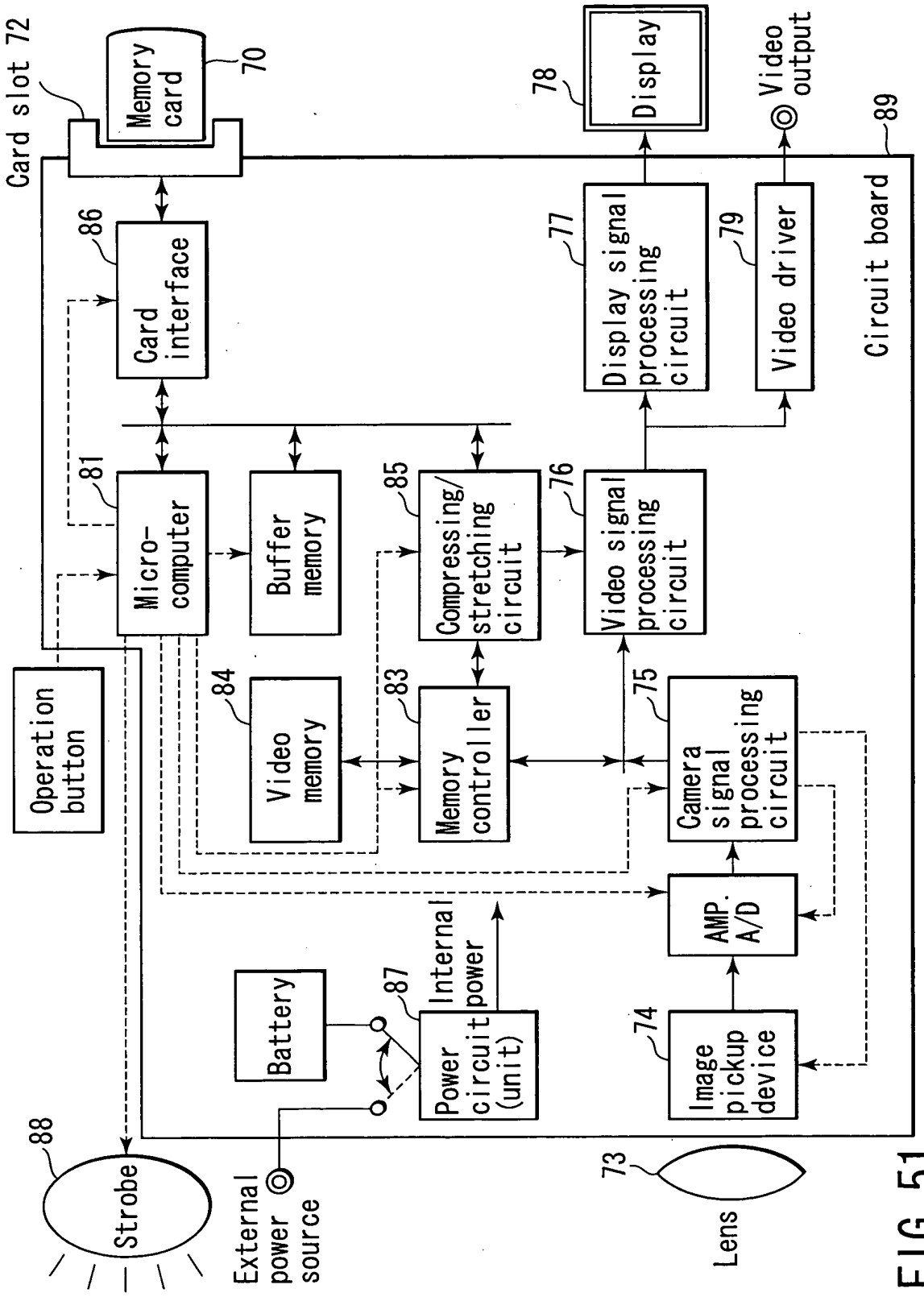

Card slot 72
Memory card
70
78
Display
Video output
89
Circuit board
86
Card interface
77
Display signal processing circuit
79
Video driver
81
Micro-computer
Buffer memory
85
Compressing/ stretching circuit
76
Video signal processing circuit
Operation button
84
Video memory
83
Memory controller
75
Camera signal processing circuit
AMP. A/D
Battery
87
Internal power
Power circuit (unit)
74
Image pickup device
88
Strobe
External power source
73
Lens

FIG. 51

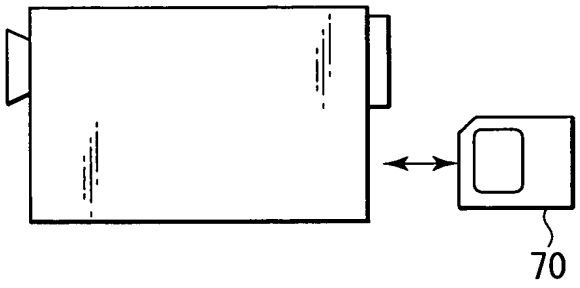


FIG. 52A

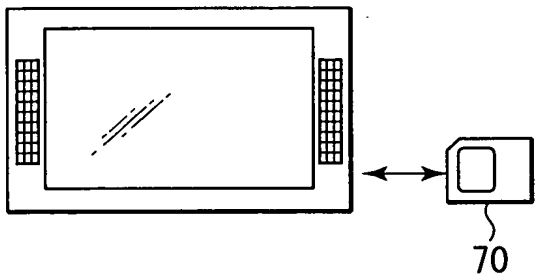


FIG. 52B

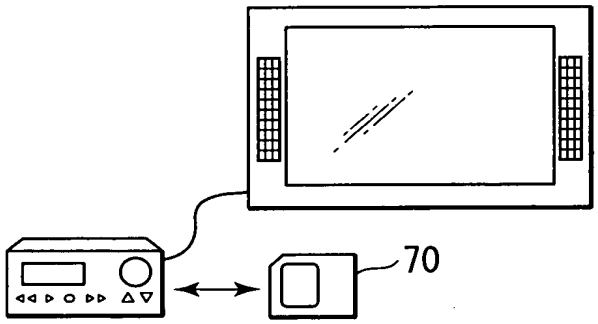


FIG. 52C

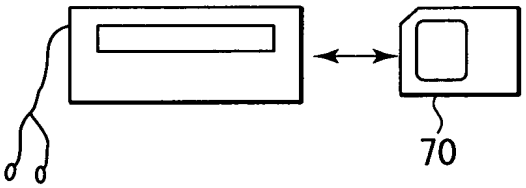


FIG. 52D

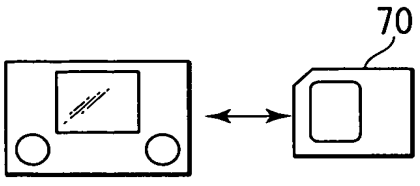


FIG. 52E

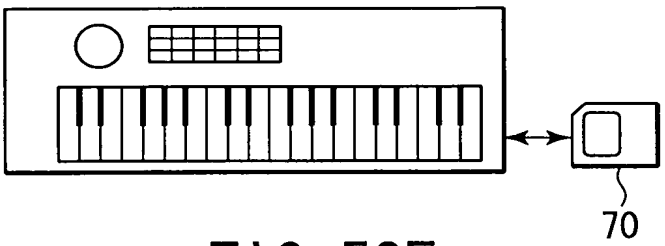


FIG. 52F

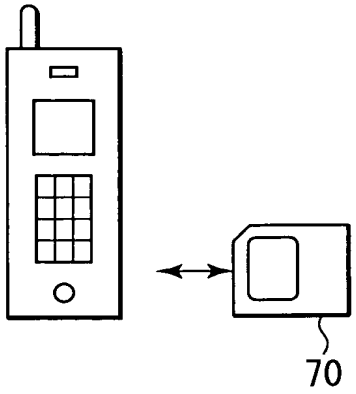


FIG. 53A

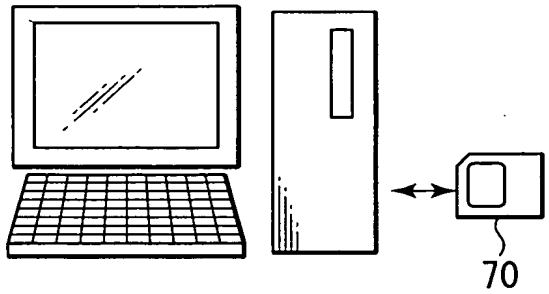


FIG. 53B

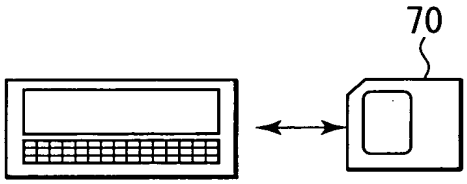


FIG. 53C

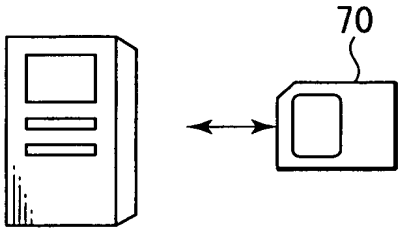


FIG. 53D

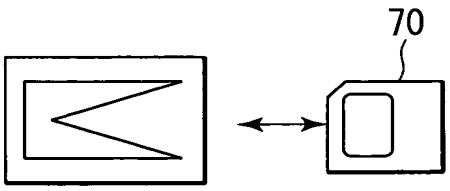


FIG. 53E

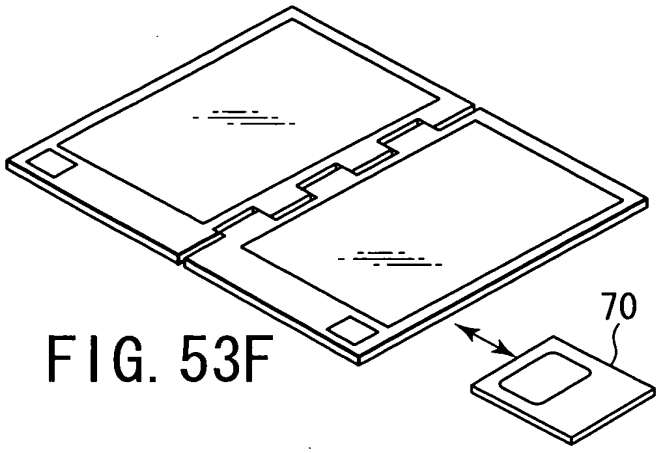


FIG. 53F